VLSI TECHNOLOGY, INC.

CATALOG PRODUCT DESCRIPTIONS

February 1987

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VLSI TECHNOLOGY, INC.

SECTION 1

INTRODUCTION

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GENERAL

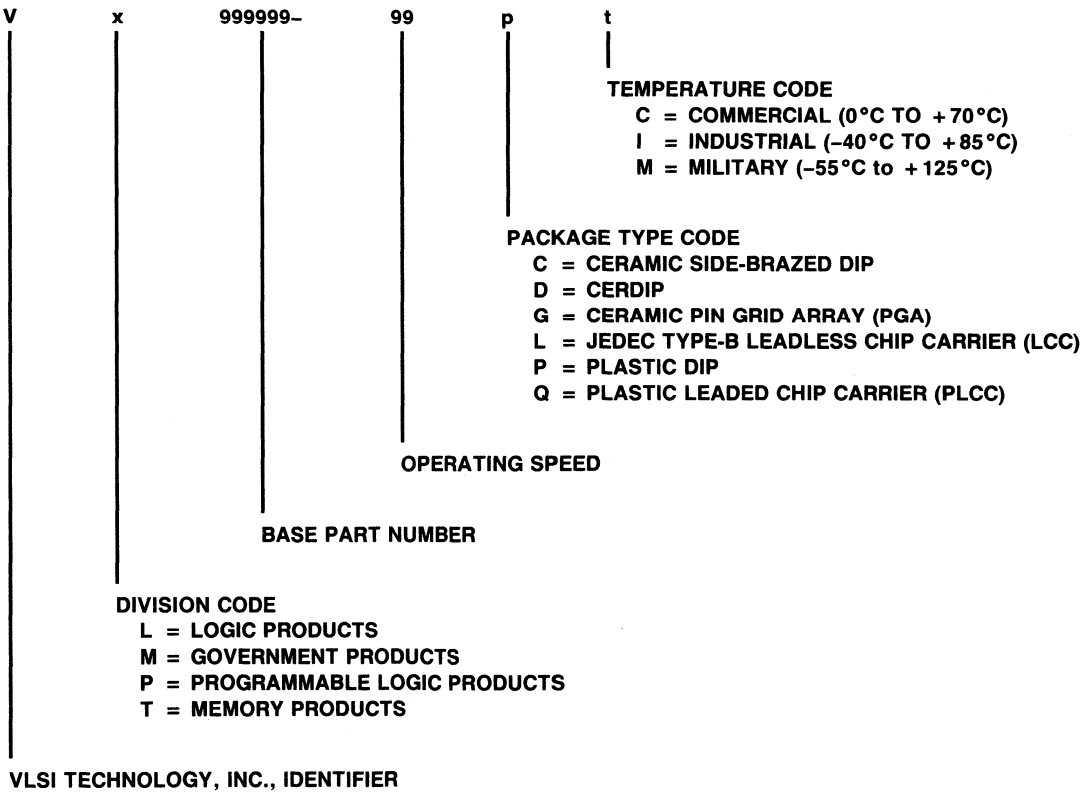
The primary business objective of VLSI Technology, Inc., (VLSI) is to provide systems designers with total application-specific integrated circuit (ASIC) solutions. To accomplish this, it has created a unique blend of expert design tools, leading-edge process technologies, state-of-the-art fabrication facilities, and a wide range of "catalog" devices. An overview of these devices is presented in this short-form catalog. More complete information can be obtained from a VLSI Technology sales office, sales representative, or distributor, or directly from the Divisions.

ORDERING INFORMATION

VLSI Technology, Inc., products are available in a variety of plastic and ceramic packages, including chip carriers and pin grid arrays, and in different temperature ranges. Specific information on the packages and temperature ranges for a particular device is coded into the part number assigned to it.

For example, the part number VL68C45R-23PC would indicate a CMOS revision R version of the 6845 CRT controller having a 2 MHz bus clock and a 3 MHz character clock, housed in a plastic DIP, operating over the commercial temperature range, and manufactured by the Logic Products Division. Similarly, the part number VT20C18-20CC would indicate a 2K x 8 16K SRAM having 20 ns access and cycle times, housed in a ceramic side-brazed DIP, operating over the commercial temperature range, and manufactured by the Memory Products Division.

PART NUMBER ORGANIZATION



VLSI TECHNOLOGY, INC.

SECTION 2

APPLICATION SPECIFIC LOGIC PRODUCTS DIVISION

Catalog
Product
Descriptions

GENERAL

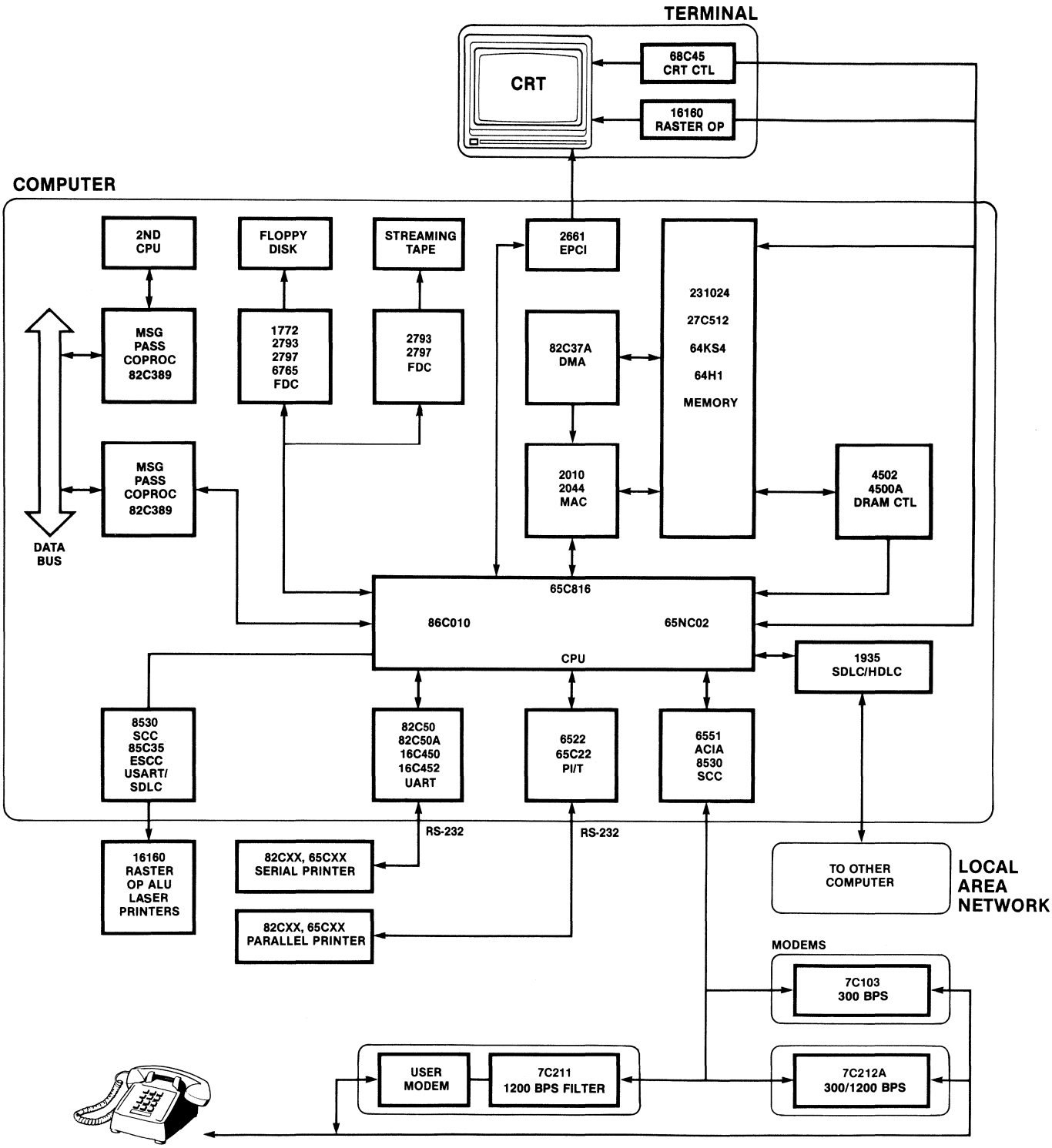
The Application Specific Logic Products Division of VLSI Technology is responsible for the manufacture and marketing of a diverse logic-based product line that encompasses both innovative and proven, well-established catalog devices. This line includes microprocessors and coprocessors, peripheral circuits, digital signal processing devices, and products for data communications and telecommunications applications.

Unlike other suppliers of such devices, however, VLSI is also a recognized leader in ASICs. As such, it not only possesses the design, process, and fabrication capabilities necessary to produce the highest quality off-the-shelf components, but is also able to treat its logic products as an integral part of a complete solution. One of the primary vehicles for accomplishing this is the megacell. The functions represented by individual devices can be implemented as megacells in VLSI's software libraries and used for semicustom circuit design, and functions developed as megacells for specific applications can be turned into catalog products.

The Logic Products Division is located at:

10220 South 51st Street
Phoenix, AZ 85044
602/893-8574

TOTAL SYSTEM SOLUTION



VLSI TECHNOLOGY, INC.

SECTION 3

PROCESSOR AND COPROCESSOR PRODUCTS

Catalog
Product
Descriptions

VL65NC02

CMOS 8-BIT MICROPROCESSOR

FEATURES

- CMOS silicon-gate technology
- Low power
  —1.1 mA/MHz
- Software-compatible with the NMOS 6502
- Single 5 V power supply required
- 8-bit parallel processing
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- Ready input
- Direct memory access (DMA) capability
- Clock speeds up to 4 MHz
- Pipelined architecture
- On-chip clock options:
  External single-input clock
  On-board clock, single external crystal

DESCRIPTION

The VL65NC02 is an 8-bit microprocessor device produced using CMOS silicon-gate technology. This device provides advanced system architecture for enhancements in system performance, speed, and value over its NMOS counterparts, the 65XX family of microprocessor devices. The VL65NC02 is the CMOS equivalent of the NMOS 6502, and contains some enhancements. This CMOS type may exhibit different intermediate cycle information from that resident in the NMOS 6502. Intermediate cycle information is not specified, and should not be used.

The VL65NC02 provides 64K bytes of addressable memory and an interrupt input, as well as options for on-chip oscillators and drivers. It is bus-compatible and software-compatible with the 65XX CPU family.

CLOCK GENERATOR

The clock generator develops all internal clock signals and (where applicable) external clock signals associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase-one clock pulse for as many cycles as are required to complete the instruction. Each data transfer that takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

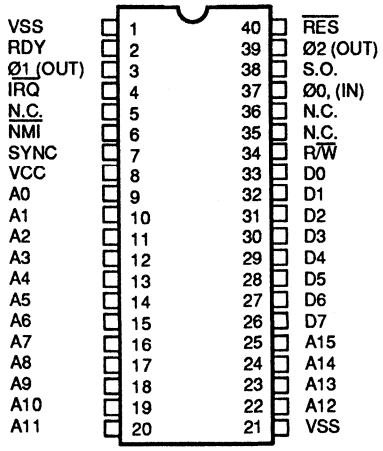
PROGRAM COUNTER

The 16-bit program counter provides the addresses that step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

PIN DIAGRAM

VL65NC02



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65NC02-01PC	1 MHz	Plastic DIP
VL65NC02-01CC		Ceramic DIP
VL65NC02-02PC	2 MHz	Plastic DIP
VL65NC02-02CC		Ceramic DIP
VL65NC02-03PC	3 MHz	Plastic DIP
VL65NC02-03CC		Ceramic DIP
VL65NC02-04PC	4 MHz	Plastic DIP
VL65NC02-04CC		Ceramic DIP

Note: Operating temperature range is 0°C to + 70°C

VL65C816•VL65C802

CMOS 16-BIT MICROPROCESSOR FAMILY

FEATURES

- Advanced CMOS design for low power consumption and increased noise immunity
- Single 3 - 6 V power supply, 5 V specified
- Emulation mode allows complete hardware and software compatibility with 6502 designs
- 24-bit address bus allows access to 16M bytes of memory space
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Valid data address (VDA) and valid program address (VPA) output allows dual cache and cycle steal DMA implementation
- Vector pull (VP) output indicates when interrupt vectors are being addressed
- VP may be used to implement vectored interrupt design
- $\overline{\text{ABORT}}$ input and associated vector supports interrupting any instruction without modifying internal registers
- Separate program and data bank registers allow program segmentation
- New Direct Register allows "zero page" addressing anywhere in first 64K bytes
- 24 addressing modes: 13 original 6502 modes plus 11 new addressing modes, with 91 instructions using 255 opcodes
- New Wait for Interrupt (WAI) and Stop the Clock (STP) instructions further reduce power consumption, decrease interrupt latency and allow synchronization with external events
- New Co-Processor (COP) instruction with associated vector supports co-processor configurations (e.g., floating point processors)

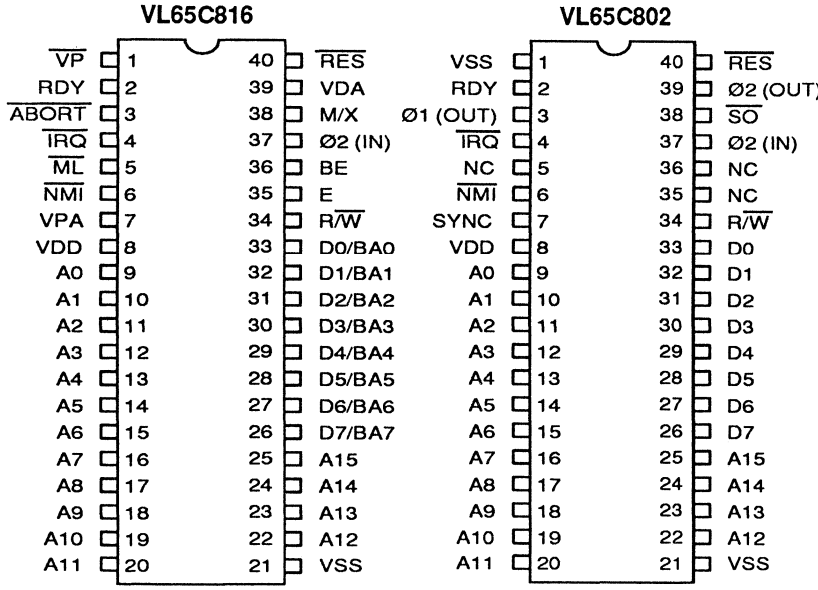
DESCRIPTION

The VL65C802 and VL65C816 are CMOS 16-bit microprocessors featuring total software compatibility with their 8-bit NMOS and CMOS 6500-series predecessors. The VL65C802 is pin-for-pin compatible with 8-bit devices currently available, while the VL65C816 extends addressing to a full 16 megabytes. These devices offer the many advantages of CMOS technology, including increased noise immunity, higher reliability, and greatly reduced power requirements. A software switch determines whether the processor is in the 8-bit "emulation" mode or in the "native" mode, thus allowing existing systems to use the expanded features.

The Accumulator, ALU, X and Y Index registers, and Stack Pointer Register have all been extended to 16 bits. A new 16-bit Direct Page Register augments the direct page addressing mode (formerly zero page addressing). Separate Program Bank and Data Bank Registers allow 24-bit memory addressing.

Four new signals provide the system designer with many options. The $\overline{\text{ABORT}}$ input can interrupt the currently executing instruction without modifying internal registers. Valid data address (VDA) and Valid program address (VPA) outputs facilitate dual cache memory by indicating whether a data segment or program segment is accessed. Modifying a vector is made easy by monitoring the vector pull (VP) output.

PIN DIAGRAMS



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65C802-02PC	2 MHz	Plastic DIP
VL65C802-02CC		Ceramic DIP
VL65C816-02PC		Plastic DIP
VL65C816-02CC		Ceramic DIP
VL65C802-04PC	4 MHz	Plastic DIP
VL65C802-04CC		Ceramic DIP
VL65C816-04PC		Plastic DIP
VL65C816-04CC		Ceramic DIP
VL65C802-06PC	6 MHz	Plastic DIP
VL65C802-06CC		Ceramic DIP
VL65C816-06PC		Plastic DIP
VL65C816-06CC		Ceramic DIP
VL65C802-08PC	8 MHz	Plastic DIP
VL65C802-08CC		Ceramic DIP
VL65C816-08PC		Plastic DIP
VL65C816-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

VL82C389

MESSAGE-PASSING COPROCESSOR MULTIBUS® II

FEATURES

- Full-function, single-chip interface to Parallel System Bus (iPSB)
- Implements full message-passing protocol on iPSB bus
- Offloads managing iPSB bus arbitration, transfer and exception cycles from local CPU
- Compatible with Bus Arbiter/ Controller (BAC) and Message Interrupt Controller (MIC) interface designs
- Maximizes performance on iPSB bus and local on-board bus
- Simplifies highly functional interconnect space implementations for both local and iPSB buses
- Processor-independent interface to iPSB bus
- Supports co-existence of dual-port and message-passing architectures

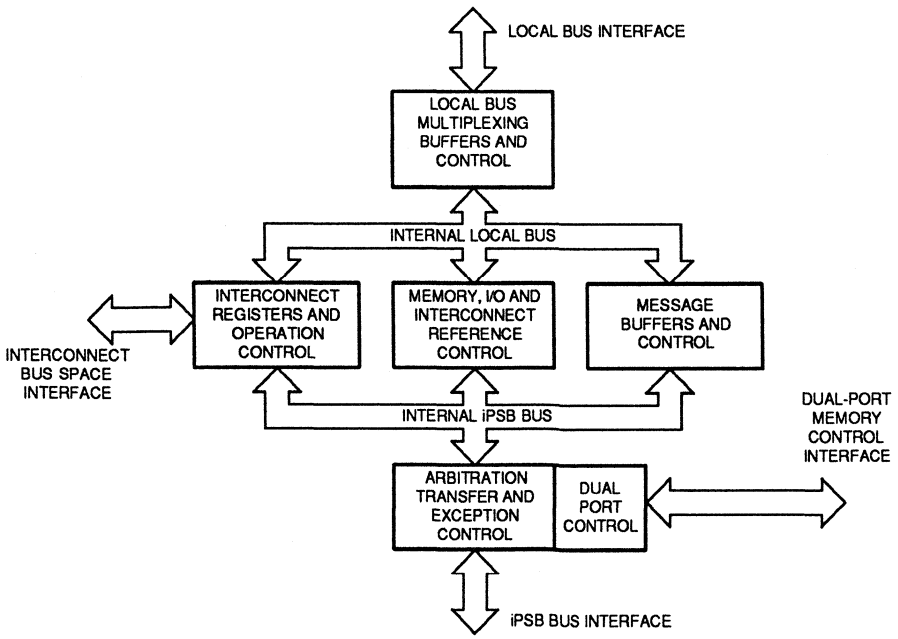
DESCRIPTION

The VL82C389 Message Passing Coprocessor (MPC) provides a high-integration interface solution for the Parallel System Bus (iPSB) of the Multibus II architecture. The device integrates the logic necessary to implement a full bus interface solution, including support for message passing and interconnect spaces, as well as memory and I/O references on the iPSB bus. In addition, the MPC is designed to simplify implementation of dual-port memory functions for those designs that must co-exist with message passing.

The message address space in the MULTIBUS II architecture has been defined to provide a high-performance interprocessor communication mechanism for multiprocessor systems. By performing the message space interface, the VL82C389 MPC offloads the interprocessor communication tasks from the local on-board CPU, which decouples the local bus activities from the iPSB bus activities. Decoupling these two functions eliminates an interface bottleneck present in traditional dual-port architectures. The bottleneck is a result of having a dual-port architecture that requires a tight coupling between a processor and some shared memory resource of limited size. Unfortunately, as the number of processors increases, the dual-port structure degrades system performance even more dramatically.

Using the MPC component to decouple these resources yields several enhancements to system performance. For example, resources on the local processor bus and parallel system bus are not held in wait states while arbitration for other resources is performed. In addition, each transfer can occur at the full bandwidth of the associated bus. The benefit of this is the increased overall system performance that results from processors being able to process other tasks in parallel, with message transfers being handled by the MPC component.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C389-GC	Ceramic Pin Grid Array (PGA)

Note: Operating temperature range is 0°C to +70°C.

® Multibus is a registered trademark of Intel Corp.

VL86C010

32-BIT RISC MICROPROCESSOR

DESCRIPTION

- 32-bit internal architecture
- 32-bit external data bus
- 64M-byte linear address space
- Bus timing optimized for standard DRAM usage with page mode operation
- 32M-byte/second bus bandwidth
- Simple/powerful instruction set providing an excellent high level language compiler target
- Hardware support for virtual memory systems
- Low interrupt latency for real-time application requirements
- Full CMOS implementation results in low power consumption
- Single 5 V ± 5% operation
- 84-pin JEDEC Type-B leadless chip carrier or plastic leaded chip carrier (PLCC)

FEATURES

The VL86C010 Acorn RISC Machine (ARM) is a full 32-bit general-purpose microprocessor designed using reduced instruction set computer (RISC) methodologies. The processor is targeted for the microcomputer, graphics, industrial and controller markets for use in stand-alone or embedded systems. Applications in which the processor is useful include laser printers, graphics engines, N.C. machines and any other systems requiring fast real-time response to external interrupt sources and high processing throughput.

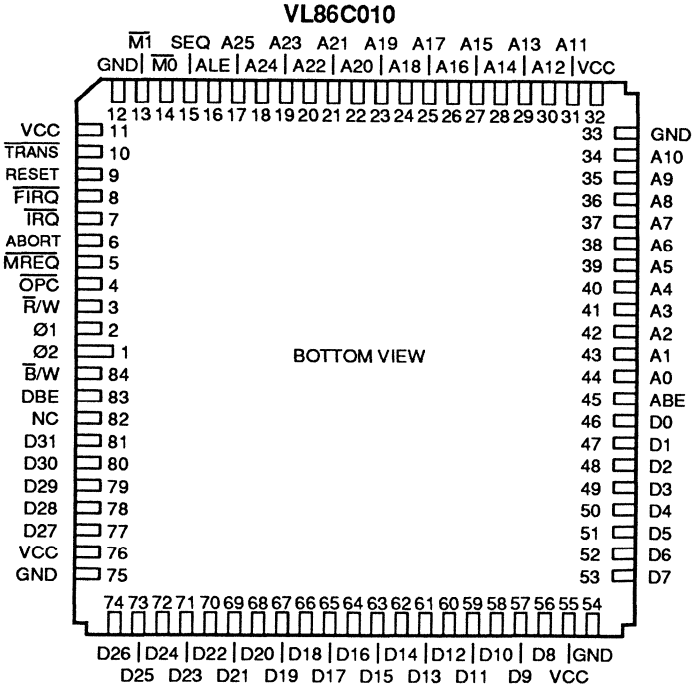
The VL86C010 features a 32-bit data bus, 25 registers of 32 bits each, a load-store architecture, a partially overlapping register set, 3 µs worst-case interrupt latency, conditional instruction execution, a 26-bit linear address space and an average instruction execution rate of from three-to-four million instructions per second (MIPS). Additionally, the processor supports two addressing modes: program counter (PC) and base register relative modes. The ability to do pre- and post-indexing allows stacks and queues to be easily implemented in software. All instructions are 32 bits long (aligned on word boundaries), with register-to-register operations executing in one cycle. The two data types supported are 8-bit bytes and 32-bit words.

Using a load-store architecture simplifies the execution unit of the processor, since only a few instructions deal directly with memory and the rest operate register-to-register. Load and store multiple register instructions provide enhanced performance, making context switches faster and exploiting sequential memory access modes.

The processsor supports two types of interrupts that differ in priority and register usage. The lowest latency is provided by the fast interrupt request (FIRQ) which is used primarily for I/O to peripheral devices. The other interrupt type (IRQ) is used for interrupt routines that do not demand low-latency service or where the overhead of a full context switch is small compared with the interrupt process execution time.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C010-04QC	4 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C010-04LC		JEDEC Type-B Ceramic Carrier
VL86C010-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C010-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 4

PERIPHERAL PRODUCTS

Catalog
Product
Descriptions

VL16160

RASTER OP ALU

FEATURES

- Provides hardware assist for bit-mapped graphics operations. Includes 32-bit barrel shifter
- Performance increase over software implementations:
  - Monochrome = 4 X Software
  - Color = 4 X (Planes) X Software
- Supports both CRT displays and such hardcopy devices as laser printers
- Compatible with both monochrome and color displays
- Implements all 256 possible raster operations on source, destination, and pattern data
- 28-pin package; 5 V supply

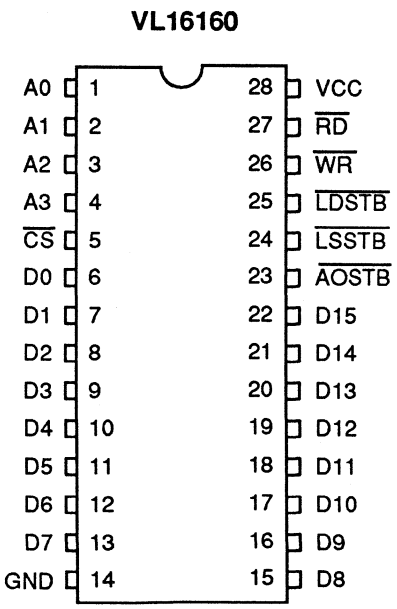
DESCRIPTION

The VL16160 Raster Op ALU (RALU) provides hardware-assisted performance enhancements for bit manipulation operations used in bit-mapped graphics displays. These operations, commonly called bit block translation (BITBLT), allow bit-mapped images to be combined and manipulated by logical operators. These operators include AND, OR, and XOR, and can be used on source, destination, and pattern data. Additionally, support for masking with multiple mask registers for clipping is included.

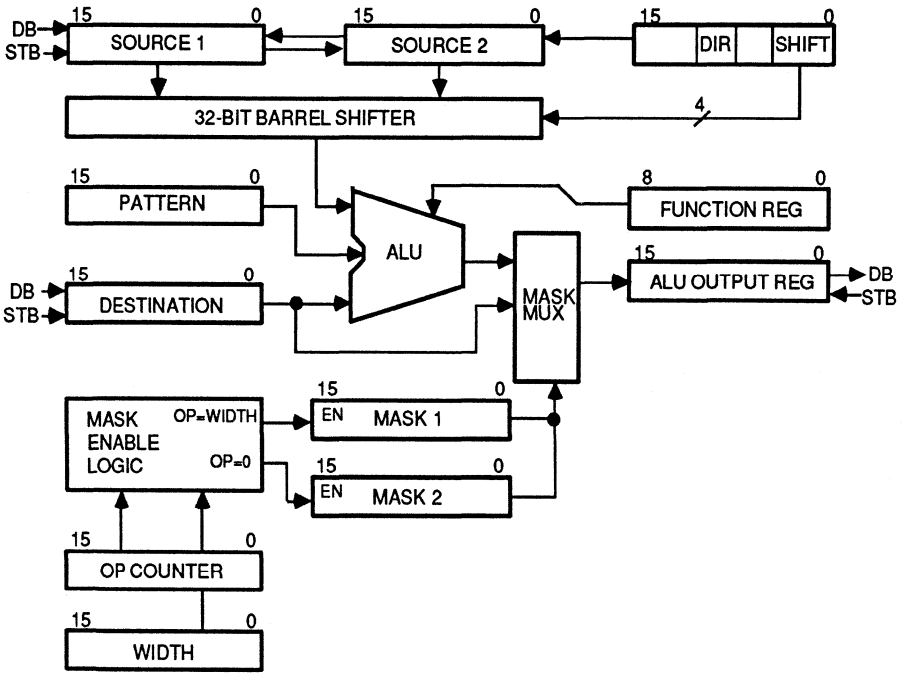
The BITBLT operation is general purpose enough to be used in a wide range of graphics operations, including text display using arbitrary fonts, attributes, and enhancements. Successive applications of BITBLT can perform such operations as scaling, filling, rotations, and texturing.

In a typical application, the RALU operates on display data in 16-bit words that are latched into its input buffers by external hardware. Once source, destination, pattern, shift, and masking data are loaded into the RALU, the source data is bit-aligned with the destination data, and the logical operation specified in the function register takes place. The results are stored in the ALU Output Register, which can be output onto the bus by a single strobe signal.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL16160-PC	Plastic DIP
VL16160-CC	Ceramic DIP
VL16160-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL1772-02

FLOPPY DISK CONTROLLER/FORMATTER

FEATURES

- Built-in data separator
- Built-in write precompensation
- Single and double density
- Motor control
- 128, 256, 512, or 1024 sector lengths
- TTL compatible
- 8-bit bidirectional data bus
- Fast step rates
- 28-pin DIP
- Single 5 V power supply

DESCRIPTION

The VL1772-02 is an MOS/LSI device that performs the functions of a 5 1/4-inch floppy disk controller/formatter. It replaces the older 1770-type device.

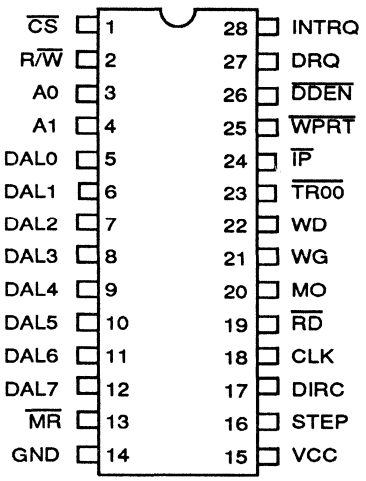
The drive side of the interface needs no additional logic except for buffers/receivers. Designed for 5 1/4-inch single- or double-density operation, the device contains a programmable Motor On signal.

The VL1772-02 is implemented in NMOS silicon-gate technology and is available in a 28-pin dual in-line package. It is a low-cost version of the WD179X Floppy Disk Controller/Formatter and is compatible with generic 179X types. It also has a built-in digital data separator and write precompensation circuits. A single read (RD) line (pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device has been specifically designed for control of floppy disk drives with data rates of 125K bps (single density) and 250K bps (double density). In addition, it can write a precompensation that is125 ns from nominal, and can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to automatically enable the spindle motor prior to operating a selected drive. The VL1772-02 offers stepping rates of 2, 3, 6, and 12 ms.

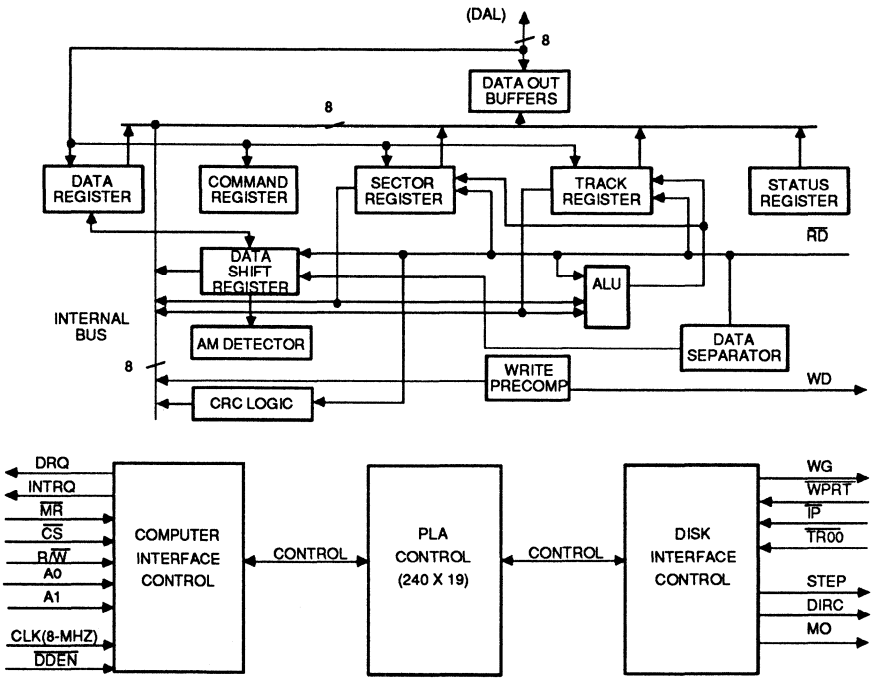
The processor interface consists of an 8-bit bidirectional bus for transfer of the status information, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three LS loads.

PIN DIAGRAM

VL1772-02



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL1772-02PC	Plastic DIP
VL1772-02QC	Plastic Leaded Chip Carrier (PLCC)
VL1772-02CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL2793 • VL2797

FLOPPY DISK FORMATTER/ CONTROLLER FAMILY

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

DESCRIPTION

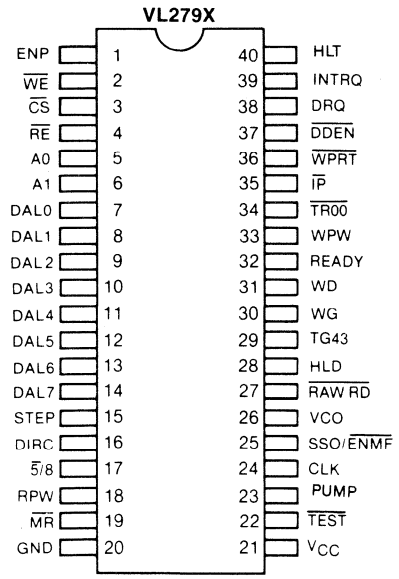
The VL279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The VL279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The VL279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and VL279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The VL279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The VL279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2797 has a side select output for controlling double-sided drives.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Format	Package
VL2793-PC VL2793-CC	Single-Sided	Plastic DIP Ceramic DIP
VL2797-PC VL2797-CC	Double-Sided	Plastic DIP Ceramic DIP

Note:
Operating temperature range: 0°C to +70°C.

VL4500A

DYNAMIC RAM CONTROLLER

FEATURES

- Controls operation of 8K/16K/32K/64K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 256K bytes of memory without external drivers
- Operates from microprocessor clock
  - — No crystals, delay lines, or RC networks
  - — Eliminates arbitration delays
- Refresh may be internally or externally initiated
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- 3-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns/250 ns
- Compatible with TI TMS 4500A

DESCRIPTION

The VL4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

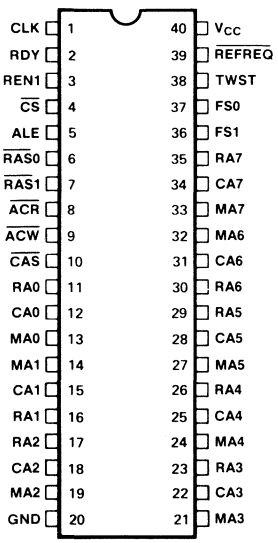
The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

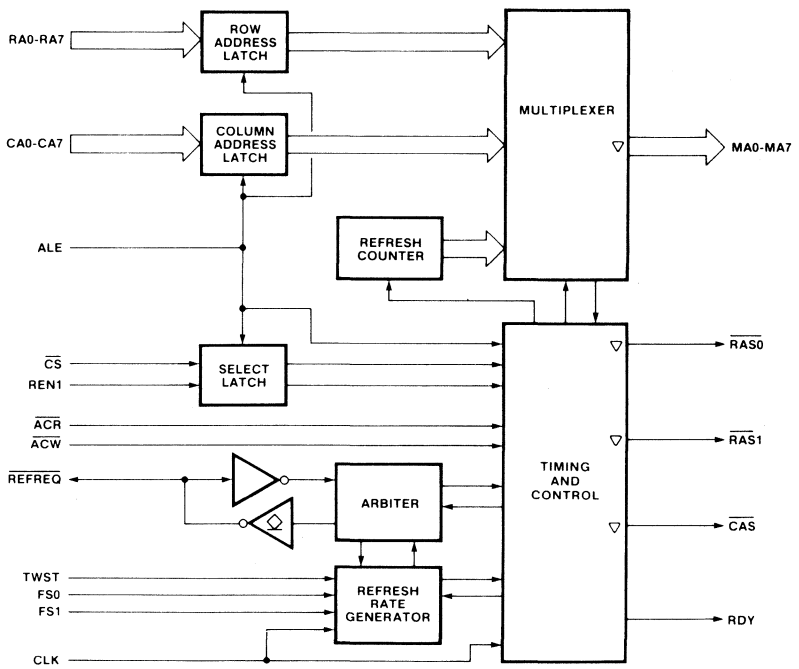
The VL4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles.

PIN DIAGRAM

VL4500A



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Access Time	Package
VL4500A-15PC VL4500A-15CC	150 ns	Plastic DIP Ceramic DIP
VL4500A-20PC VL4500A-20CC	200 ns	Plastic DIP Ceramic DIP
VL4500A-25PC VL4500A-25CC	250 ns	Plastic DIP Ceramic DIP

Note:
Operating temperature range: 0°C to +70°C.

VLSI TECHNOLOGY, INC.

VL4502

DYNAMIC RAM CONTROLLER

FEATURES

- Inputs are TTL voltage compatible
- Controls operation of 64K and 256K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 2 megabytes of memory without external drivers
- Operates from microprocessor clock
  - —No crystals, delay lines, or RC networks
  - —Eliminates arbitration delays
- Refresh may be internally or externally initiated
- High performance CMOS technology
- Strap-selected wait state generation for microprocessor/ memory speed matching
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- 3-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns
- Compatible with VLSI VL4500A and TI TMS4500A, THCT4502

DESCRIPTION

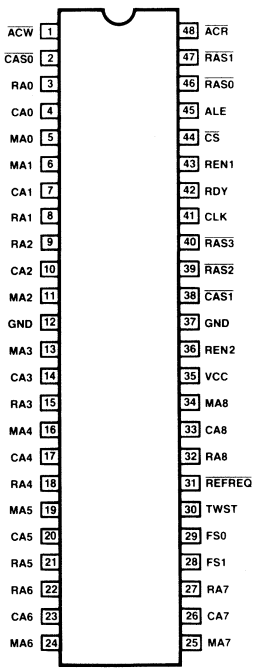
The VL4502 is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

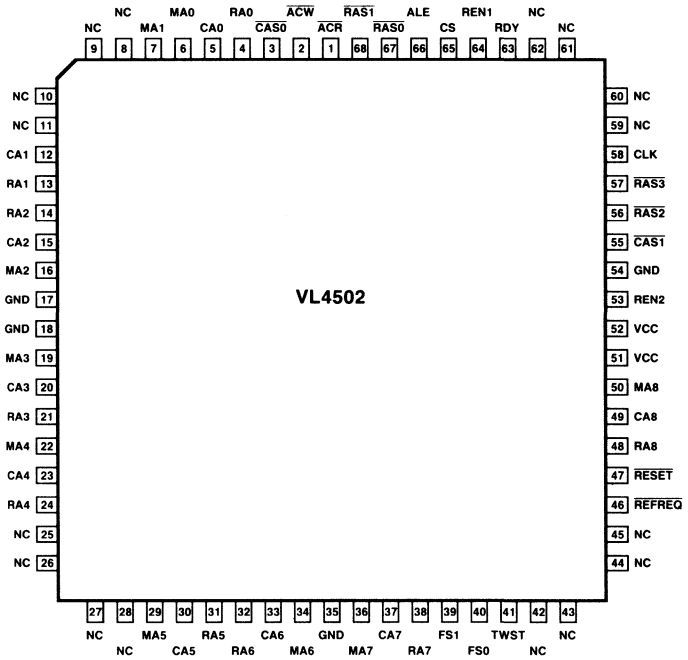
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

PIN DIAGRAMS

VL4502 DIP





ORDER INFORMATION

Part Number	Access Time	Package
VL4502-15PC	150 ns	Plastic DIP
VL4502-15CC		Ceramic DIP
VL4502-15QC		Plastic Leaded Chip Carrier (PLCC)
VL4502-20PC	200 ns	Plastic DIP
VL4502-20CC		Ceramic DIP
VL4502-20QC		Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

VL6522•VL65C22

PARALLEL INTERFACE/TIMER

FEATURES

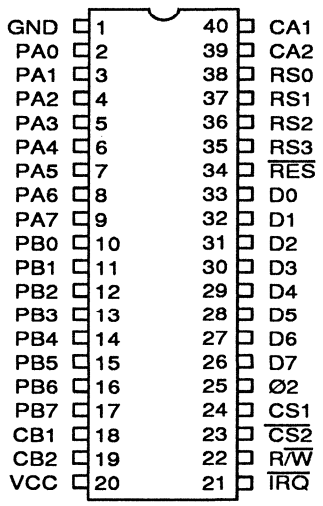
- Low-power consuming CMOS parallel interface/timer (VL65C22)
- Low-cost HMOS parallel interface/timer (VL6522)
- Two 8-bit bidirectional I/O ports
- Two 16-bit timer/counters
- Serial bidirectional peripheral I/O port
- Enhanced handshake features
- Programmable Data Direction Registers
- TTL compatible I/O peripheral lines

DESCRIPTION

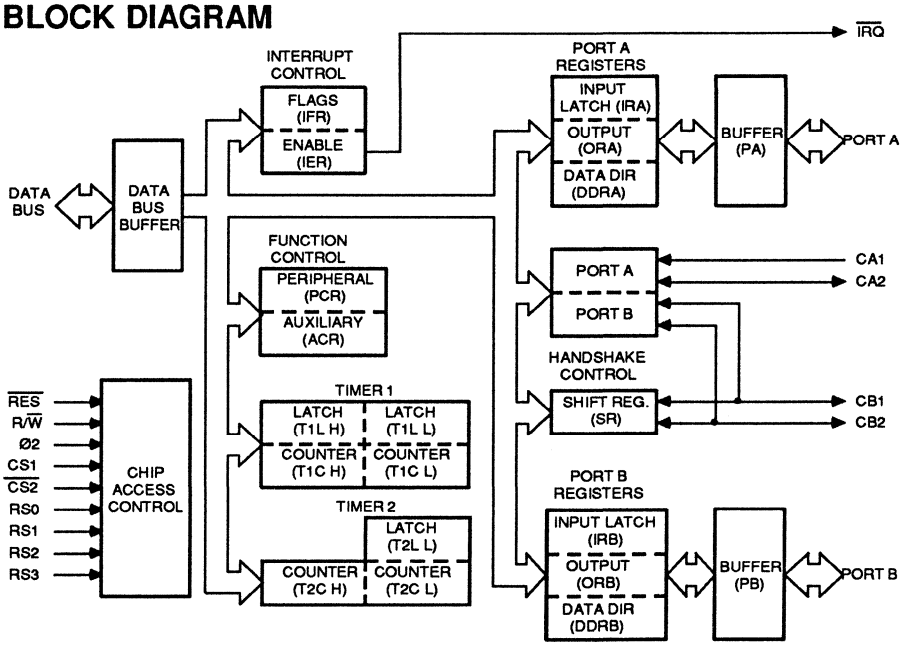
The VL6522/VL65C22 are flexible I/O devices for use with the 65XX family of processors. The VL65C22 is a CMOS implementation of the VL6522 device. Both include functions for programmed control of up to two peripheral devices (ports A and B). Two program-controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral devices. Two programmable Data Direction Registers (A and B) allow selection of data direction (input versus output) on an individual line-by-line basis. Also provided are two programmable 16-bit counter/timers with latches. Timer 1 may be operated in a one-shot interrupt mode with interrupts on each count-to-zero, or in a free-running mode with a series of evenly spaced interrupts. Timer 2 functions both as an interval and pulse counter. Serial data transfers are provided by a shift register. Application versatility is further increased by various control registers, including an interrupt flag register, an interrupt enable register, and two function control registers.

PIN DIAGRAM

VL6522
VL65C22



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Technology	Clock Frequency	Package
VL6522-01PC	HMOS	1 MHz	Plastic DIP
VL65C22-01PC	CMOS		Plastic DIP
VL6522-01QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-01QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL6522-02PC	HMOS	2 MHz	Plastic DIP
VL65C22-02PC	CMOS		Plastic DIP
VL6522-02QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-02QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-03PC	CMOS	3 MHz	Plastic DIP
VL65C22-03QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-04PC	CMOS	4 MHz	Plastic DIP
VL65C22-04QC	CMOS		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL6765

DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

FEATURES

- Address mark detection circuitry
- Software control of
  —Track stepping rate
  —Head load time
  —Head unload time
- IBM compatible in both single- and double-density format
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- Replaces the NEC μPD765A, Intel 8272A, and Rockwell 6765A
- Single phase 4 or 8 MHz clock
- Single +5 volt power supply

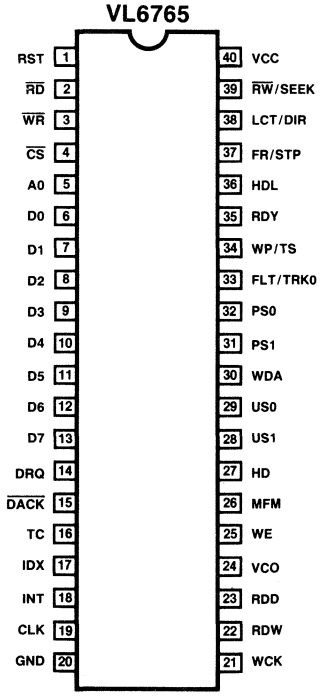
DESCRIPTION

The VL6765 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z80, 8080A, 8085A, 8086, and 8088. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The VL6765 is directly compatible with the Z8410/μPD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL6765-04PC VL6765-04CC VL6765-04QC	4 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL6765-08PC VL6765-08CC VL6765-08QC	8 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

VL6845R/E • VL68C45R/S

VL6845 CRT CONTROLLER FAMILY AND VMC68C45 MEGACELL DESIGN KIT

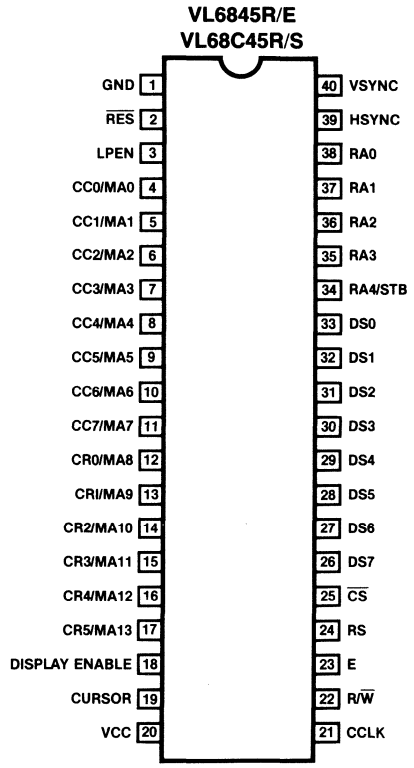
FEATURES

- CRT Controller Family—
  Rev E compatibility with SY6845E
  Rev R compatibility with MC6845
  CMOS versions available:
  CMOS Rev R compatible with MC6845R1, MC6845 and MC146845 CMOS Rev S compatible with HD6845S
- Internal refresh address generation
- Character clocks up to 5 MHz
- Bus clocks up to 3 MHz

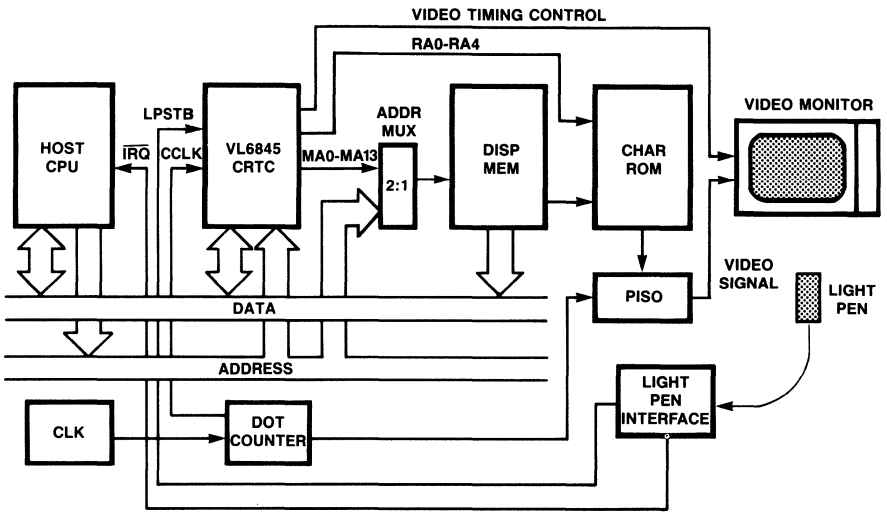
DESCRIPTION

The VL6845X and VL68C45X are a family of CRT controllers that are widely used in both bit-mapped and character-mapped applications for both terminals and personal computers. The VL6845 family offers compatibility with the Motorola family of HMOS controllers while the VL68C45 family allows designs to consume less power through the use of CMOS technology. In addition to compatibility with both the Motorola and Hitachi families, the VL68C45R also contains enhancements found in the MC6845R1. These enhancements allow for higher resolution displays without extra external hardware.

PIN DIAGRAM



SYSTEM DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency		Part Number	Clock Frequency		Package
	Bus	Character		Bus	Character	
VL6845R-23 VL68C45R-23 VL68C45S-23	2 MHz	3 MHz	VL6845E-33 VL6845R-33 VL68C45R-33 VL68C45S-33	3 MHz	3 MHz	To specify package type, add the appropriate suffix to the part number: PC = Plastic DIP CC = Ceramic DIP QC = Plastic Leaded Chip Carrier (PLCC)
VL6845E-24 VL6845R-24 VL68C45R-24 VL68C45S-24		4 MHz	VL6845E-34 VL6845R-34 VL68C45R-34 VL68C45S-34		4 MHz	
			VL6845R-35 VL68C45R-35 VL68C45S-35		5 MHz	

Note: Operating temperature range: 0°C to +70°C.

VL82C284

CMOS CLOCK GENERATOR AND INTERFACE

FEATURES

- Generates clock for Intel 286-type microprocessor-based systems
- External TTL source or crystal may be used as frequency source.
  — On-board crystal oscillator
- Provides READY signal for system synchronization
- Generates system reset
- Schmitt trigger reset input assures stability and noise immunity
- Low power consuming CMOS technology
- Single 5 V power supply required

DESCRIPTION

The VL82C284 is a clock generator and driver that provides clock and interface signals to Intel 286-type microprocessor-based systems. All device output signals are synchronized to the output clock signal.

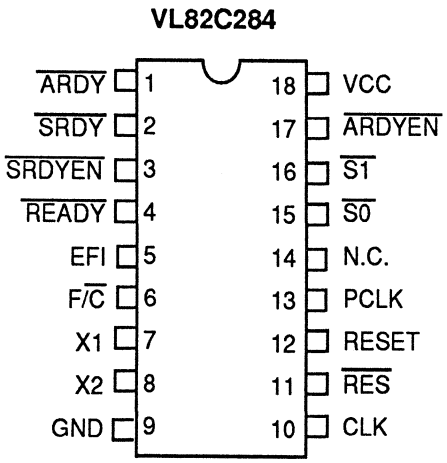
The clock input and output frequencies are twice the frequency used internally by the microprocessor in the system. To avoid confusion, the clock frequency in the order information represents the internal system microprocessor clock frequency (e.g., the devices listed as 8 MHz would actually have an input crystal or a TTL signal frequency of 16 MHz).

The VL82C284 also supplies the system with a high-noise-immunity reset, as well as a synchronous peripheral clock and a synchronous READY to indicate the completion of the current bus cycle.

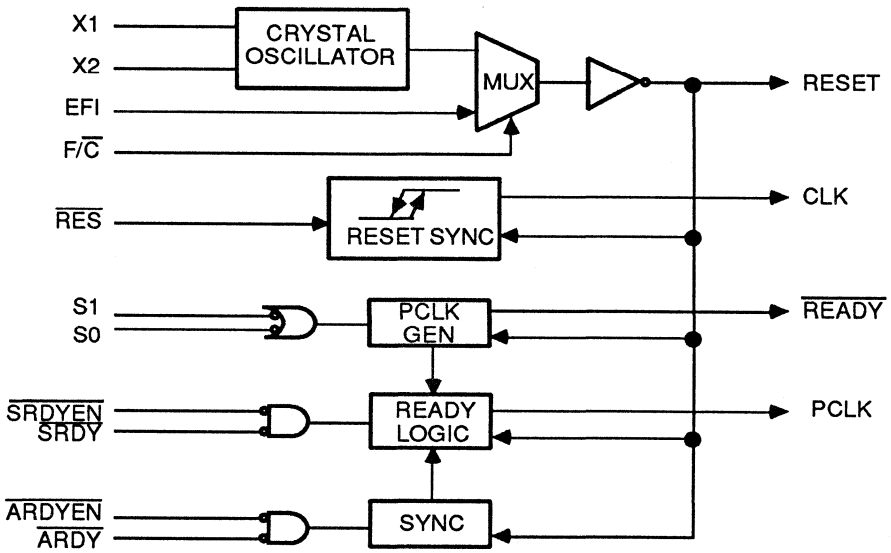
The peripheral clock is controlled by two status input signals, which may be left open if not used.

The VL82C284 is available in an 18-pin ceramic and plastic DIP, as well as in a plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C284-06PC	6 MHz	Plastic DIP
VL82C284-06QC		Plastic Leaded Chip Carrier (PLCC)
VL82C284-06CC		Ceramic DIP
VL82C284-08PC	8 MHz	Plastic DIP
VL82C284-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C284-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL82C288

CMOS BUS CONTROLLER

FEATURES

- Both local and system bus commands and control are provided
- Supports both Multibus® and high-speed bus cycle operating modes
- High-current output drivers
- Flexible command timing
- High degree of system configuration flexibility
- Low power consuming CMOS technology
- Single 5 V power supply

DESCRIPTION

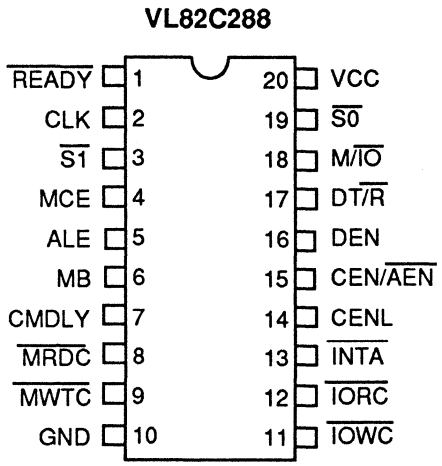
The VL82C288 is a CMOS bus controller for use in Intel 286-type microprocessor-based systems. A mode select pin allows strapping the device for Multibus operation or for short bus cycles. The device also provides separate command outputs for memory and I/O devices. The data bus is controlled by separate data direction and data enable signals.

A system clock provides the timing control required by the microprocessor-based system. The device clock input is twice the system clock speed. To avoid confusion, the clock frequency listed in the order information is the system clock frequency (e.g., the devices listed as 8 MHz Clock Frequency, would have an input clock of 16 MHz).

The VL82C288 meets the timing and drive requirements to satisfy the IEEE-796 standard for Multibus.

The VL82C288 is available in a 20-pin ceramic or plastic DIP, as well as in a plastic leaded chip carrier.

PIN DIAGRAM



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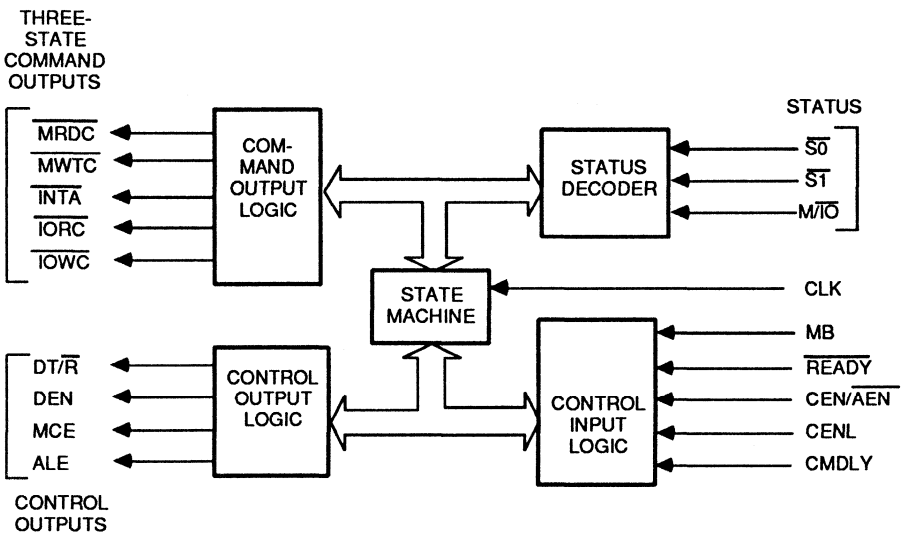


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C288-06PC	6 MHz	Plastic DIP
VL82C288-06QC		Plastic Leaded Chip Carrier (PLCC)
VL82C288-06CC		Ceramic DIP
VL82C288-08PC	8 MHz	Plastic DIP
VL82C288-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C288-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL82C37A

CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- High performance 8 MHz version available
- Transfers may be terminated by end-of-process input
- Software-controlled DMA requests
- Independent polarity control for DREQ and DACK signals

DESCRIPTION

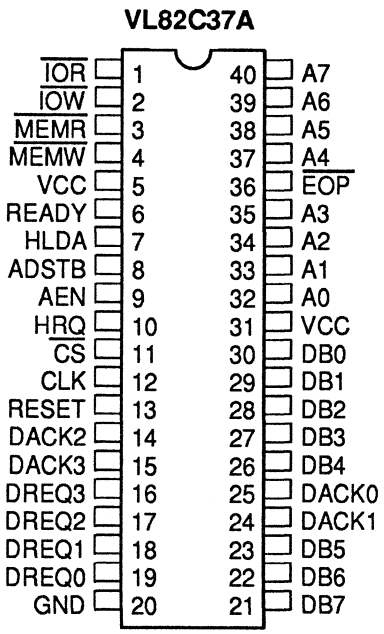
The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

The VL82C37A is designed to be used with an external 8-bit address register such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an end-of-process (EOP) input. Each channel also has a 64K address and word count handling ability.

The VL82C37A DMA Controller is available in 5 MHz and 8 MHz clock frequencies.

PIN DIAGRAM



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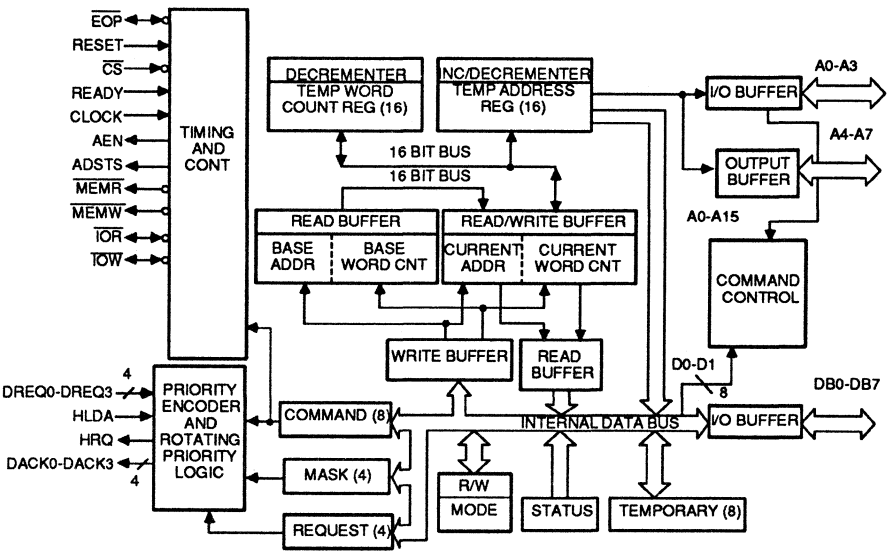


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C37A-05PC	5 MHz	Plastic DIP
VL82C37A-05CC		Ceramic DIP
VL82C37A-05QC		Plastic Leaded Chip Carrier (PLCC)
VL82C37A-08PC	8 MHz	Plastic DIP
VL82C37A-08CC		Ceramic DIP
VL82C37A-08QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL82C54

PROGRAMMABLE INTERVAL TIMER

FEATURES

- Compatible with 8080A, 8085A, 8088, 8086, and similar microprocessors
- Counts in binary or BCD
- Clock inputs from dc to maximum clock operating frequency
- Status may be readback on command
- Single 5 V power supply
- Three independent 16-bit counters
- Six programmable counter modes
- Low power consuming CMOS technology

DESCRIPTION

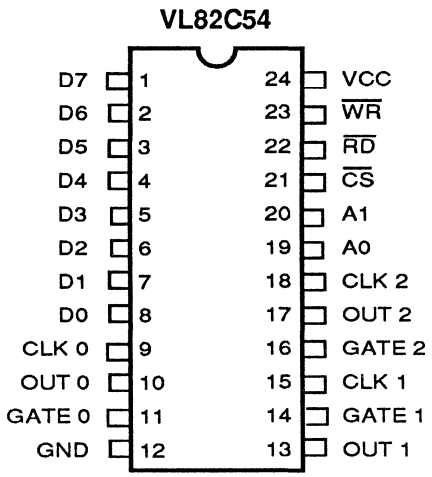
The VL82C54 is a CMOS programmable interval timer/counter designed for use with Intel-type microcomputer systems. It is a general-purpose, multi-timing element that can be considered as three separate counters by the system software.

The VL82C54 solves the problem of generating an accurate timing interval in the microprocessor-based system. Instead of setting up timing loops in software, the programmer configures the VL82C54 to generate the timing intervals required by the system. At the termination of the delay, the VL82C54 generates an interrupt to the CPU. The overhead software is minimal, and variable lengths are easily programmed.

In addition to the three independent 16-bit counters, the VL82C54 also has its own 8-bit data bus, two address lines, a chip select, and individual read and write control lines.

The VL82C54 is available in 8 MHz and 10 MHz maximum clock frequencies.

PIN DIAGRAM



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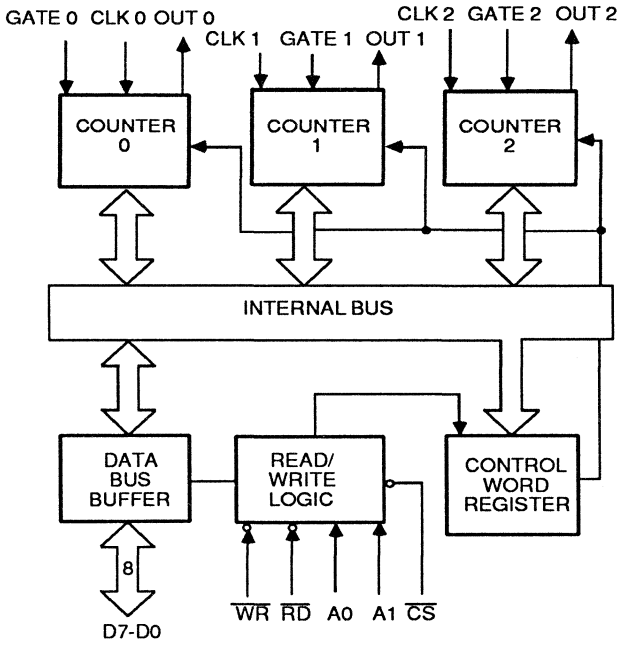


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C54-08PC	8 MHz	Plastic DIP
VL82C54-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C54-08CC		Ceramic DIP
VL82C54-10PC	10 MHz	Plastic DIP
VL82C54-10QC		Plastic Leaded Chip Carrier (PLCC)
VL82C54-10CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL82C59A

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- Compatible with 8086, 8088, and similar microprocessors
- Low power consuming CMOS
- Interrupt modes are programmable
- Minimizes software overhead
- Eight prioritized control levels
- 64 levels of expandability
- Single 5 V power supply
- 28-pin DIP Package

DESCRIPTION

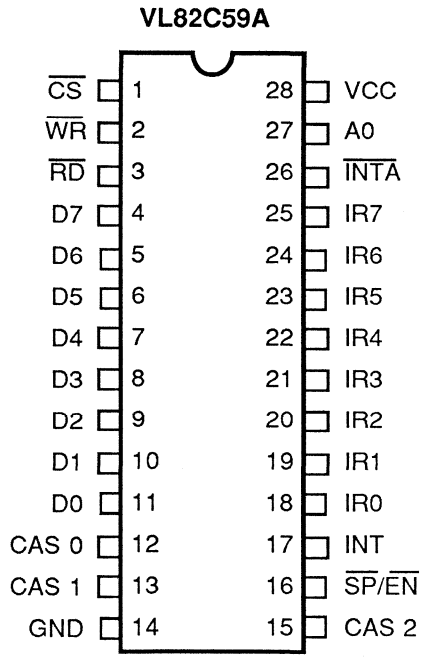
The VL82C59A Programmable Interrupt Controller can manage up to eight vectored priority interrupts for the system's CPU. It can be cascaded to handle up to 64 interrupts. No additional circuitry is required.

The VL82C59A has been designed to relieve the software of the burden of handling multi-level priority interrupts. It controls several modes, permitting optimization for a large number of system needs.

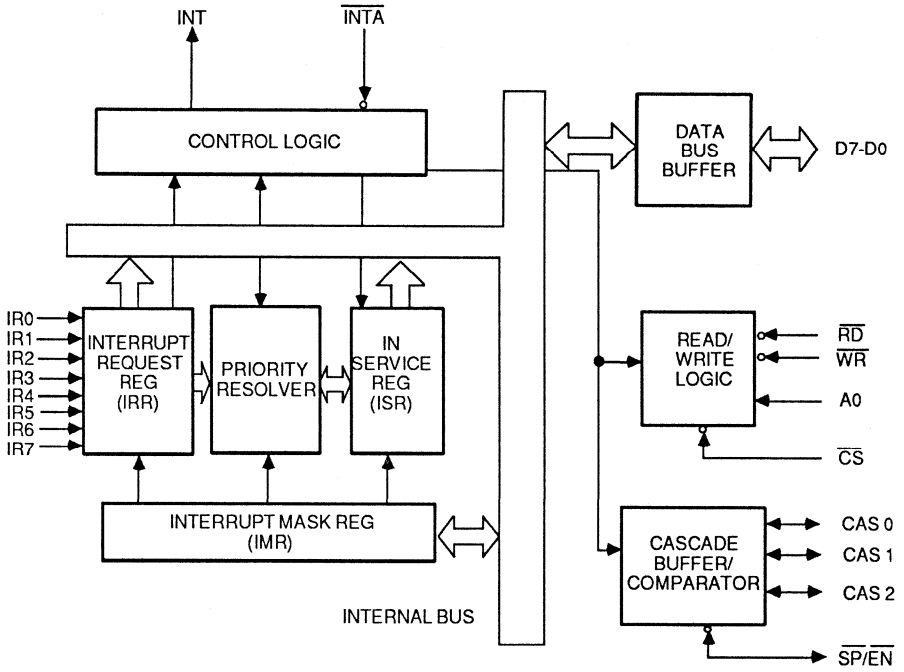
The VL82C59A is fully upward compatible with the HMOS 8259 or 8259A. Software originally written for the HMOS 8259 or 8259A will operate the VL82C59A in all 8259 or 8259A equivalent modes.

The VL82C59A is housed in a 28-pin DIP, uses CMOS technology and requires a single 5 V supply. The circuit is totally static, requiring no clock input.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Bus Speed	Package
VL82C59A-05PC	5 MHz	Plastic DIP
VL82C59A-05QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-05CC		Ceramic DIP
VL82C59A-08PC	8 MHz	Plastic DIP
VL82C59A-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL82C84A

CLOCK GENERATOR AND DRIVER

FEATURES

- Two maximum clock frequencies available
  - — 8 MHz (VL82C84A-08)
  - —10 MHz (VL82C84A-10)
- Local READY is provided, as well as Multibus® READY synchronization
- Schmitt trigger input generates system RESET output
- Clock generator supports the 8086, 8088, and other similar processors
- Capable of clock synchronization with other VL82C84A devices
- Crystal or TTL input may be used as a frequency source
- 100 mW maximum power dissipation

DESCRIPTION

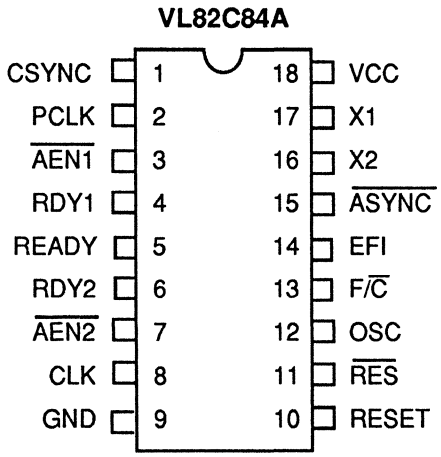
The VL82C84A is a single-chip clock generator/driver for the 8086, 8088, and similar processors. The device contains a crystal-controlled oscillator, a divide-by-three counter, and complete synchronization and reset logic. Handling all of these functions on a single device allows the VL82C84A to significantly reduce the chip count in a system, while enhancing reliability, production ease, and increasing mean time between failure (MTBF).

Fabricated in low-power CMOS, the VL82C84A provides a convenient way to decrease power consumption of the system. Fully compatible with existing designs using the NMOS 8284A, the VL82C84A provides a low-power, cost-effective solution.

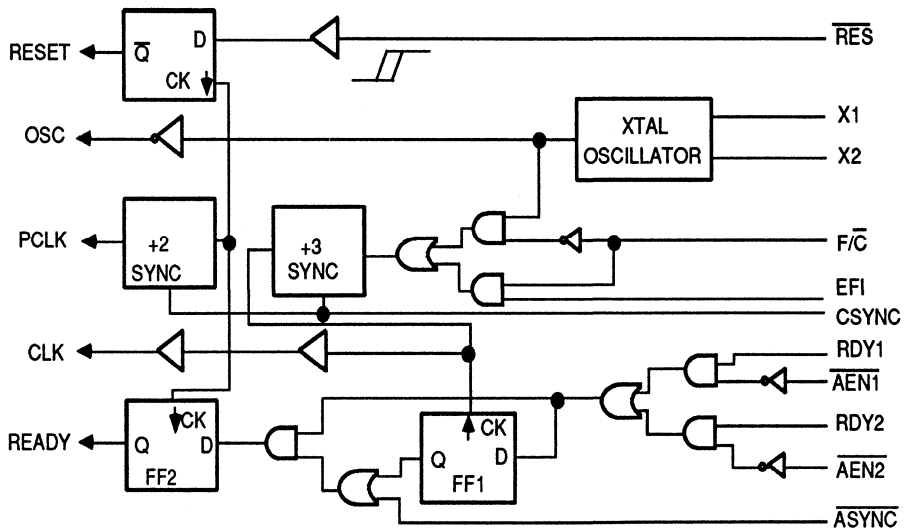
The output drivers of the VL82C84A offer driving capability of the conventional HMOS device. As a result, they do not require any external drivers.

The VL82C84A is compatible with all the other members of the VL82CXX family of microprocessor peripherals. Offering higher performance and lower power consumption than previously available 82CXX peripherals, these devices offer CMOS advantages to 8086, 8088, and similar systems.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C84A-PC	Plastic DIP
VL82C84A-QC	Plastic Leaded Chip Carrier (PLCC)
VL82C84A-CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

Multibus® is a registered trademark of Intel Corporation.

VL82C88

CMOS BUS CONTROLLER

FEATURES

- Compatible with 8086, 8088 and similar microprocessors
- Three-state command output drivers
- Low-power CMOS technology
- Fully compatible with HMOS 8288
- Advanced commands provided
- Wide flexibility in system configurations
- Can be used with an I/O Bus
- Interface to up to two multi-master buses
- Single 5 V power supply

DESCRIPTION

The VL82C88 Bus Controller is a CMOS device intended for use with medium-to-large 8086 and 8088-type microprocessor-based systems. The bus controller provides command and control timing generation as well as bus drive capability for optimizing system performance. The VL82C88 decodes the three status lines from the system microprocessor to generate the command and control signals at the specified time.

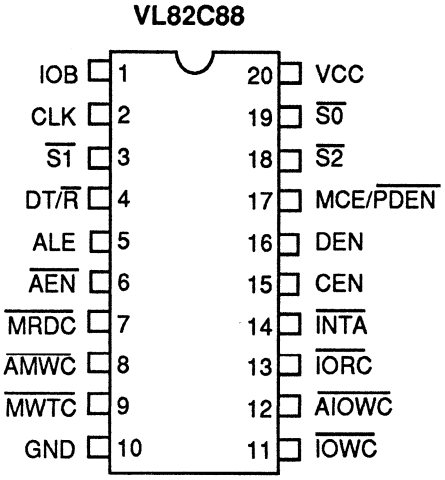
The VL82C88 bus controller generates commands in two ways:

I/O Bus Mode - The VL82C88 is in the I/O bus mode if the IOB pin is tied high. In the I/O bus mode, all I/O command lines (IORC, IOWC, AIOWC, INTA) are always enabled.

System Bus Mode - The VL82C88 is in the system bus mode if the IOB pin is tied low. In this mode, no command is issued until 115 ns after the AEN line is activated.

The 20-pin, low-power-consuming, CMOS VL82C88 is available with a 10 MHz clock frequency.

PIN DIAGRAM



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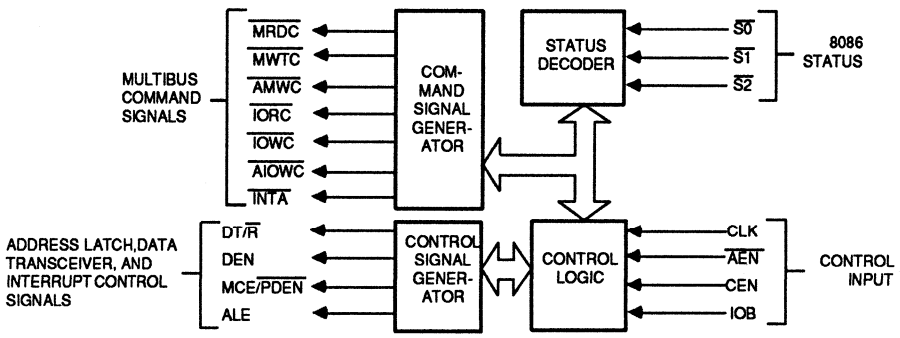


ORDER INFORMATION

Part Number	Package
VL82C88-PC	Plastic DIP
VL82C88-QC	Plastic Leaded Chip Carrier (PLCC)
VL82C88-CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

Multibus® is a registered trademark of Intel Corp.

VL85C81

CMOS CLOCK GENERATOR AND CONTROLLER

FEATURES

- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output
- Oscillator input frequency sources can be either crystals or external oscillators
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs
- Can be used as a general-purpose clock generator
- Single 5 V power supply
- Provides ability to stretch High and/or Low phase of clock signal under external control
- On-chip reset logic

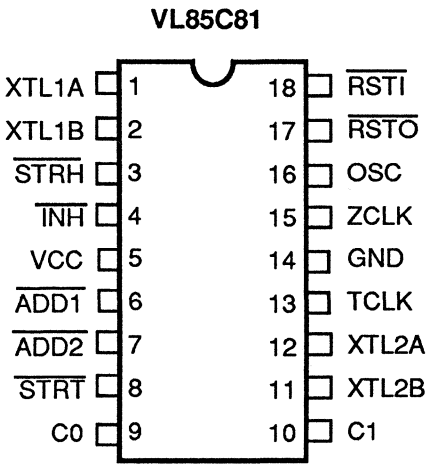
DESCRIPTION

The VL85C81 Clock Generator and Controller has selective clock-stretching capabilities and a variety of timing outputs that allow it to easily meet the timing design requirements of systems with microprocessors and peripheral devices. The clock output drivers of the VL85C81 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The VL85C81 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

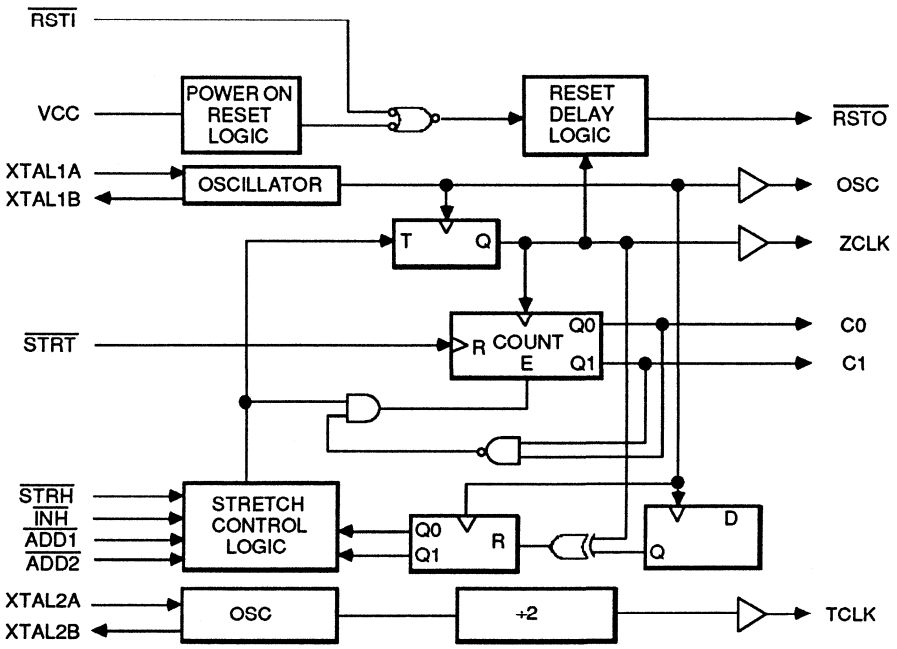
The VL85C81's oscillators are referenced to the system clock oscillator and the general-purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

A reset output (RST0) of the clock generator allows the the VL85C81's system clock output to be synchronized with an incoming reset. The external reset initiates the reset output or system reset for a minimum of 30 ms, allowing a "power up" system initialization.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C81-05PC	5 MHz	Plastic DIP
VL85C81-05QC		Plastic Leaded Chip Carrier (PLCC)
VL85C81-05CC		Ceramic DIP
VL85C81-08PC	8 MHz	Plastic DIP
VL85C81-08QC		Plastic Leaded Chip Carrier (PLCC)
VL85C81-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 5

SIGNAL PROCESSING PRODUCTS

Catalog
Product
Descriptions

VL2010

16 x 16 PARALLEL MULTIPLIER-ACCUMULATOR

FEATURES

- 16 x 16 parallel multiplication and product accumulation
- High-speed multiply-accumulate time
  —65 ns, typical
  —90 ns, max
- CMOS silicon-gate technology
- Low power
  —0.2 W typical
- Single 5 V supply
- Standard TTL-compatible I/O levels
- Performs double-precision subtraction, addition, and multiplication, including rounding control
- Pin-for-pin functional replacement for WTL1010, WTL2010, TRW TDC1010J, LMA1010, and AMD 29510
- 64-pin ceramic and plastic DIP
- 68-terminal plastic leaded chip carrier

DESCRIPTION

The VL2010 is a 16 x 16 parallel multiplier-accumulator (MAC) fabricated using CMOS silicon-gate technology. The VL2010 offers ultra-low power and very high performance. The high performance is achieved through the use of the efficient Booth's algorithm and advanced VLSI processing technology.

The VL2010 operates from a single 5 V supply and is compatible with standard TTL logic levels. The VL2010 is a pin-for-pin functional replacement for the WTL1010, WTL 2010, TRW TDC1010J, LMA1010, and AMD 29510.

The VL2010, under control of the ACC input, performs either the multiply only, or the multiply-accumulate function. In either mode, input data X and Y can be specified as two's complement or unsigned magnitude. Input data representation is selectable via the input control line, TC. In the multiply-only mode, extended product (XTP) data is sign-extended or set to zero for two's complement and unsigned-magnitude arithmetic, respectively. Additionally, a RND control is available for rounding up the most significant product (MSP)

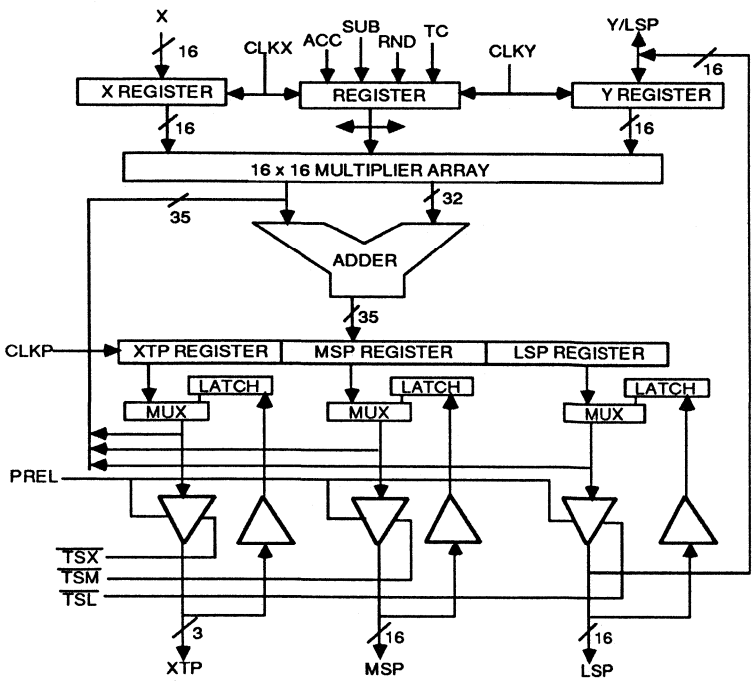
and extended product (XTP) data. In the multiply-accumulate mode, the double-precision accumulated answer is rounded back to single-precision or single-precision plus XTP bits.

The VL2010 architecture includes input and output data registers, as well as 3-state output data buses with independent, non-registered control. Time-multiplexing is used for the common least significant product (LSP) and Input Data (Y) I/O lines. Input lines $\overline{TSX}$, $\overline{TSM}$, and $\overline{TSL}$, respectively, control the outputs of the XTP, MSP, and LSP registers.

In the multiply-accumulate mode (ACC active), output data can be added to or subtracted from the last product. When SUB is also active, subtraction is performed. Otherwise, addition is performed.

The VL2010 can be efficiently applied in a variety of digital signal processing functions, including digital filtering (recursive, non-recursive, wave) and FFT processing (complex multiplication, butterfly computation). In addition, the VL2010 can be employed effectively in upgrading the computational capability of mini- and microcomputer systems.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Multiply/ Accumulate Time	Package
VL2010-65CC	90 ns	Ceramic DIP
VL2010-65PC		Plastic DIP
VL2010-65QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL2044

16 x 16 PARALLEL MULTIPLIER-ACCUMULATOR

FEATURES

- 16 x 16 parallel multiplication and product accumulation
- High speed multiply-accumulate time
  - —65 ns, typical
  - —90 ns, max
- CMOS silicon-gate technology
- Low power
  - —0.2 W typical
- Single 5 V supply
- Standard TTL-compatible I/O levels
- Performs double-precision subtraction, addition, and multiplication, including rounding control
- With the exception of preload function, pin-for-pin functional replacement for WTL1010, WTL2010, TRW TDC1010J, LMA1010, and AMD 29510
- Pin-for-pin replacement for WTL2044
- 64-pin ceramic and plastic DIP
- 68-terminal plastic leaded chip carrier
- Pin-for-pin replacement for WTL2044

DESCRIPTION

The VL2044 is a 16 x 16 parallel multiplier-accumulator (MAC) fabricated using CMOS silicon-gate technology. The VL2044 offers ultralow power and very high performance. The high performance is achieved through the use of the efficient Booth's algorithm and advanced VLSI processing technology.

The VL2044 operates from a single 5 V supply and is compatible with standard TTL logic levels. Except for the preload function, the VL2044 is a pin-for-pin functional replacement for the WTL1010, WTL 2010, TRW TDC1010J, LMA1010, and AMD 29510.

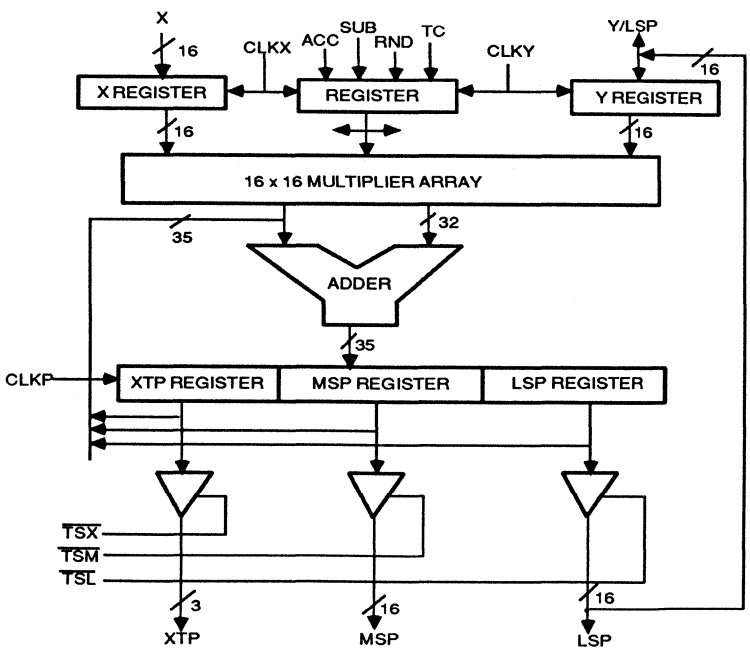
The VL2044, under control of the ACC input, performs either the multiply-only or the multiply-accumulate function. In either mode, input data X and Y can be specified as two's complement or unsigned magnitude. Input data representation is selectable via the input control line, TC. In the multiply-only mode, extended product (XTP) data is sign-extended or set to zero for two's complement and unsigned-magnitude arithmetic, respectively. Additionally, a RND control is available for rounding up the most significant product (MSP) and extended product (XTP) data. In the multiply-accumulate mode, the double-precision accumulated answer is rounded back to single-precision or single-precision plus XTP bits.

The VL2044 architecture includes input and output data registers, as well as 3-state output data buses with independent, non-registered control. Time-multiplexing is used for the common least significant product (LSP) and Input Data (Y) I/O lines. Input lines $\overline{TSX}$, $\overline{TSM}$, and $\overline{TSL}$, respectively, control the outputs of the XTP, MSP, and LSP registers.

In the multiply-accumulate mode (ACC active), output data can be added to or subtracted from the last product. When SUB is also active, subtraction is performed. Otherwise, addition is performed.

The VL2044 can be efficiently applied in a variety of digital signal processing functions, including digital filtering (recursive, non-recursive, wave) and FFT processing (complex multiplication, butterfly computation). In addition, the VL2044 can be employed effectively in upgrading the computational capability of mini- and microcomputer systems.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Multiply/ Accumulate Time	Package
VL2044-65CC	90 ns	Ceramic DIP
VL2044-65PC		Plastic DIP
VL2044-65QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 6

DATA COMMUNICATIONS PRODUCTS

Catalog
Product
Descriptions

VLSI TECHNOLOGY, INC.

VL16C450 • VL82C50A • VL82C50

ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Modem control signals include $\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$.
- Programmable serial interface characteristics:
  - —5-,6-,7- or 8-bit characters
  - —Even-, odd- or no-parity bit generation and detection
  - —1-, 1½- or 2-stop bit generation
  - —Baud rate generation (dc to 56K baud)
- Full status reporting capabilities
- 3-state TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTION

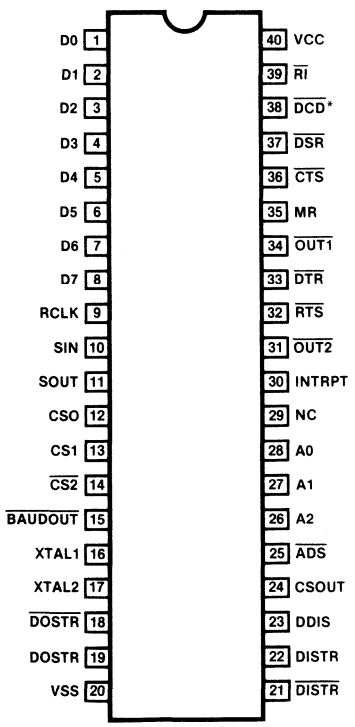
The VL16C450 is an asynchronous communications element (ACE) that is functionally equivalent to the VL82C05A, but is an improved-specification version of that part. The improved specifications provide ensured compatibility with state-of-the-art CPUs.

The VL16C450, VL82C50A, and VL82C50 ACEs serve as serial data input/output interfaces in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}-1).

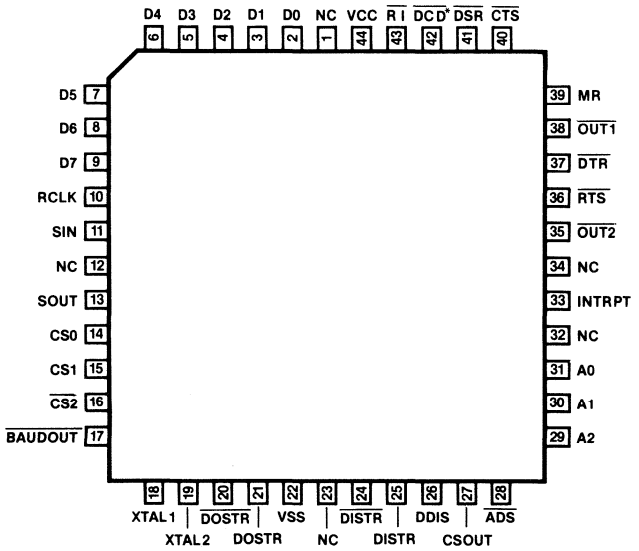
PIN DIAGRAMS

VL16C450
VL82C50A
VL82C50



*ON THE VL82C50, PIN 38 (PIN 42 ON THE PLCC PACKAGE) IS ALSO CALLED $\overline{RLSD}$

VL16C450
VL82C50A
VL82C50



ORDER INFORMATION

Part Number	Maximum External Clock Frequency	Package
VL16C450-PC	3.1 MHz	Plastic DIP
VL16C450-CC		Ceramic DIP
VL16C450-QC		Plastic Leaded Chip Carrier (PLCC)
VL82C50A-PC	3.1 MHz	Plastic DIP
VL82C50A-CC		Ceramic DIP
VL82C50A-QC		Plastic Leaded Chip Carrier (PLCC)
VL82C50-PC	3.1 MHz	Plastic DIP
VL82C50-CC		Ceramic DIP
VL82C50-QC		Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

VL16C452

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Dual-function version of VL16C450
- Centronix printer interface
- Full double buffering on both channels
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - —5-,6-,7- or 8-bit characters
  - —Even-, odd- or no-parity bit generation and detection
  - —1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive capabilities for bidirectional data bus and control bus on each channel

DESCRIPTION

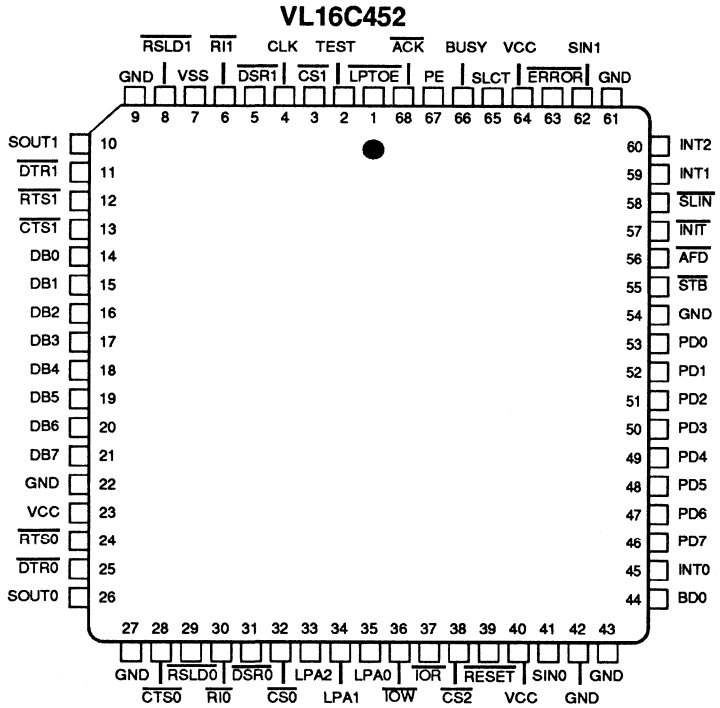
The VL16C452 is an enhanced dual-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and error conditions involving parity, overrun, framing or break interrupt.

In addition to its dual communications interface capabilities, the VL16C452 provides the user with a fully bi-directional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the dual ACE.

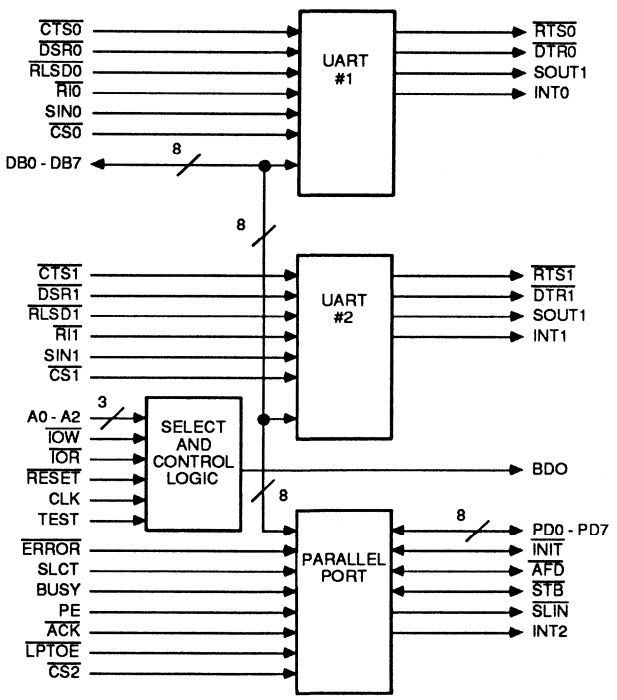
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}-1).

The VL16C452 is housed in a 68-terminal plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum External Clock Frequency	Package
VL16C452-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL1935

SYNCHRONOUS DATA LINE CONTROLLER

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING
- PIN-COMPATIBLE REPLACEMENT FOR WD1933 AND WD1935

DESCRIPTION

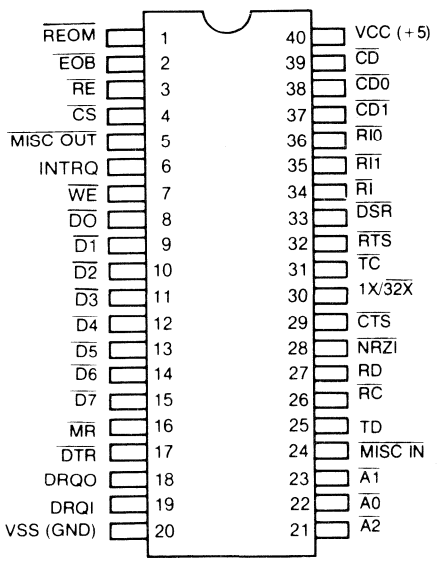
The VL1935 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. VL1935 can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL1935-10PC VL1935-10CC VL1935-10QC	0.5 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-11PC VL1935-11CC VL1935-11QC	1.0 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-12PC VL1935-12CC VL1935-12QC	1.5 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-13PC VL1935-13CC VL1935-13QC	2.0 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

VL2123

DUAL ENHANCED UNIVERSAL COMMUNICATIONS ELEMENT (DEUCE)

FEATURES

- Two independent, asynchronous, full-duplex data communication channels
- Two independent baud rate generators (one per channel)
- Each channel has the following features:
  - — Selectable 5-to-8 bit characters
  - — 1x, 16x, 64x clock rates
  - — 16 selectable baud rate clock frequencies (internal)
  - — Line break detection and generation
  - — 1, 1 1/2, or 2 stop bit selection
  - — False start bit detection
  - — Odd or even parity generation and detection
  - — Overrun and framing detection
  - — Double buffering of data
  - — TTL-compatible inputs and outputs
  - — Compatible with 8251A (async only)
  - — Diagnostic local loopback mode
  - —RXD initialization upon master reset
  - — On-board oscillator for ease of use with a crystal

DESCRIPTION

The VL2123 Dual Enhanced Universal Communications Element (DEUCE) is a single-chip MOS/LSI data communications controller circuit that contains two independent full-duplex asynchronous receiver/transmitter channels and two independent baud rate generators. The VL2123 is fabricated in N-channel silicon-gate technology and is packaged in a 40-pin plastic or ceramic DIP. All inputs and outputs are TTL-compatible.

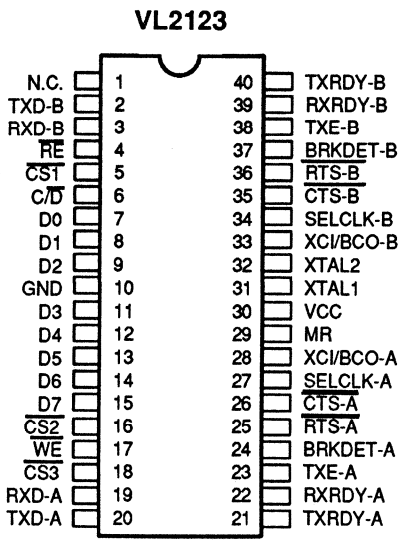
The VL2123 is a merging of two communications devices on one piece of silicon: an asynchronous-only version of the 8251A and a baud rate generator. In this manner, 8251A compatibility is maintained with the VL2123, including the added features of two channels and two baud rate generators on a single chip.

The channels are referred to as channels A and B. Channel A, which is an asynchronous 8251A, is addressed or controlled by the CS1 input signal. Channel B is similarly controlled by CS2. The baud rate generators are controlled by CS3.

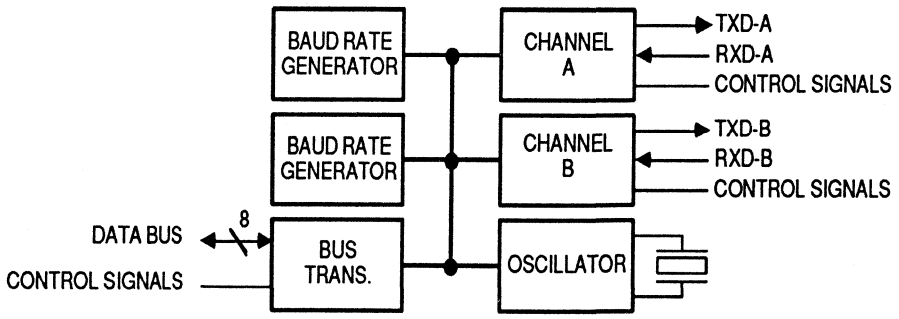
Each channel of the VL2123 can be programmed to receive and transmit asynchronous serial data. The VL2123 performs serial-to-parallel conversion on data characters received from an input/output device or modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information, reported on a per-channel basis, includes the type and the condition of the transfer operations being performed by the VL2123, as well as any transmission error conditions (parity, overrun, or framing). Programming the VL2123 is identical to the 8251A in the asynchronous mode (CS1, when low, selects channel A; when CS2 is low, it selects channel B).

The VL2123 baud rate generators may be selected either internally or externally. The clock select (CS) logic includes a clock select control bit in each Command Instruction Register. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, SELCLK, and the external clock input/baud clock output pin, XCI/BCO. When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, XCI/BCO, (SELCLK is low).

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL2123-PC	Plastic DIP
VL2123-CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL2661

ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE

FEATURES

SYNCHRONOUS OPERATION

- 5- to 8-bit characters plus parity
- Internal or external character synchronization
- Odd, even or no parity
- Local or remote maintenance loop back mode
- Baud rate: DC to 1 Mbps (1x clock)

ASYNCHRONOUS OPERATION

- 5- to 8-bit characters plus parity
- 1-, 1 1/2- or 2-stop bits transmitted
- Parity, overrun and framing error detection
- Line break detection and generation
- Local or remote maintenance loop back mode
- Baud rate: DC to 1 M bps (1x clock) —DC to 15.625 K bps (64x clock)

OTHER FEATURES

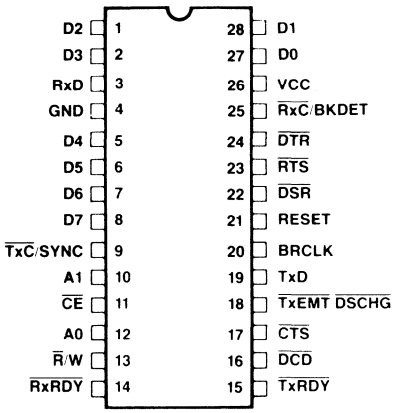
- 16 internal rates for each set
- Double-buffered transmitter and receiver
- Dynamic character length switching

DESCRIPTION

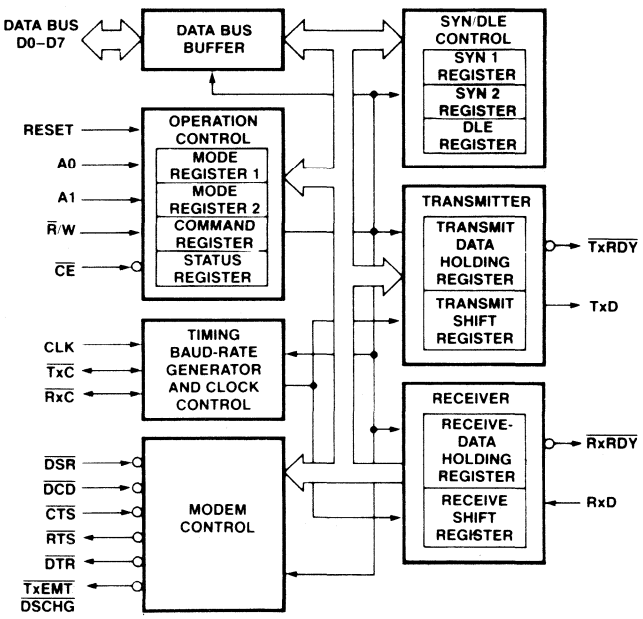
The VL2661 Enhanced Programmable Communications Interface (EPCI) is a programmable microprocessor peripheral which provides a bidirectional interface for data interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications, and provides the data formatting and control to interface serial asynchronous communication with bus-organized systems.

PIN DIAGRAM

VL2661



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Baud Rate	Clock Frequency	Package
VL2661-01PC VL2661-01CC VL2661-01QC	19.2 K	4.9152 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL2661-02PC VL2661-02CC VL2661-02QC	38.4 K		Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL2661-03PC VL2661-03CC VL2661-03QC	19.2 K	5.0688 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

VL8530

SERIAL COMMUNICATIONS CONTROLLER (SCC)

FEATURES

- Two independent full-duplex channels
- 0 to 1.5M bit/second
- Multi-protocol operation for NRZ, NRZI, or FM
- Asynchronous mode includes 1, 1.5, or 2 stop bits per character.
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Synchronous support includes internal or external character synchronization.

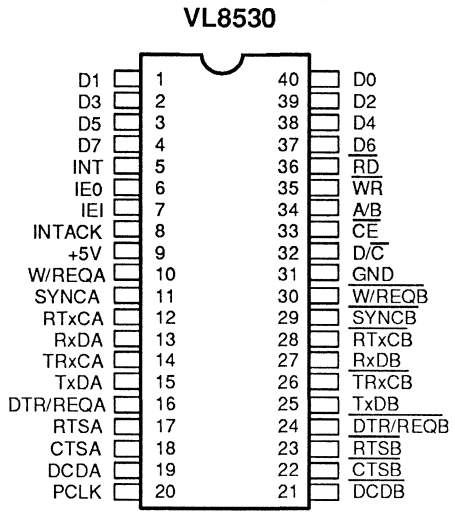
DESCRIPTION

The VL8530 Serial Communications Controller (SCC) is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators that dramatically reduce the need for external logic.

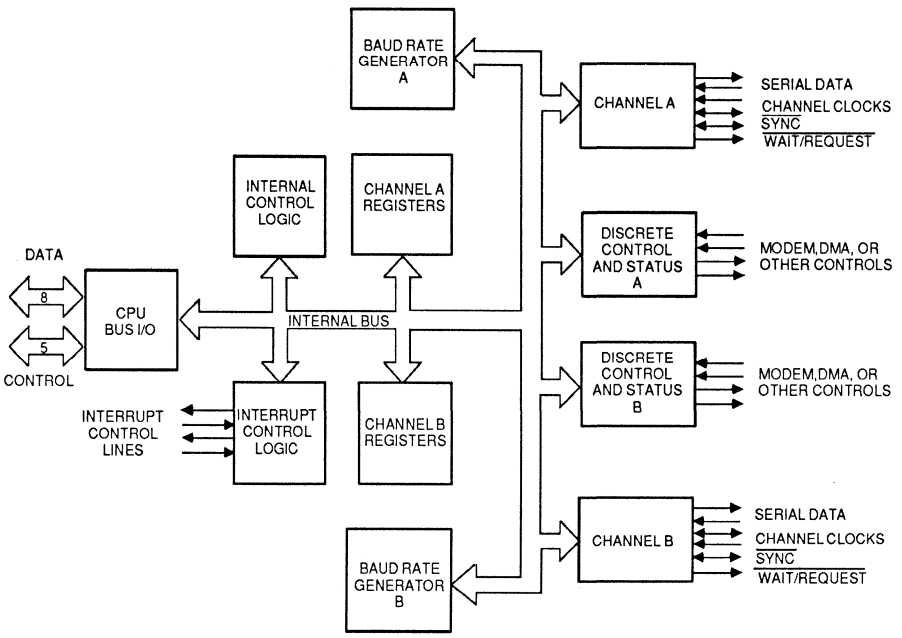
The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL8530-04PC	4MHz	Plastic DIP
VL8530-04QC		Plastic Leaded Chip Carrier (PLCC)
VL8530-04CC		Ceramic DIP
VL8530-06PC	6MHz	Plastic DIP
VL8530-06QC		Plastic Leaded Chip Carrier (PLCC)
VL8530-06CC		Ceramic DIP

Note: Operating temperature range is 0° to +70°C.

VL85C35

ENHANCED SERIAL COMMUNICATIONS CONTROLLER (ESCC)

FEATURES

- Enhanced SCC functions support DMA
  - — 14-bit byte counter
  - — 19-bit-wide FIFO
- Completely downward-compatible with the NMOS 8530
- Two independent full-duplex channels
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Internal or external character synchronization
- Low power consuming CMOS

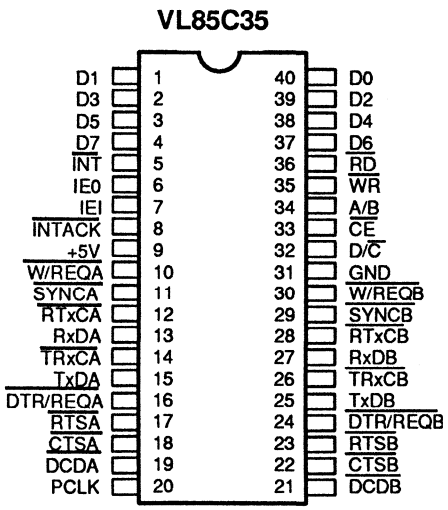
DESCRIPTION

The VL85C35 CMOS Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with non-multiplexed buses. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including all of the features of the NMOS 8530. In addition, the VL85C35 Enhanced SCC contains a 10 x 19-bit FIFO array and 14-bit byte counter. These features, in addition to the new higher clock frequency capabilities, allow the ESSC to be used with a direct memory access (DMA) controller.

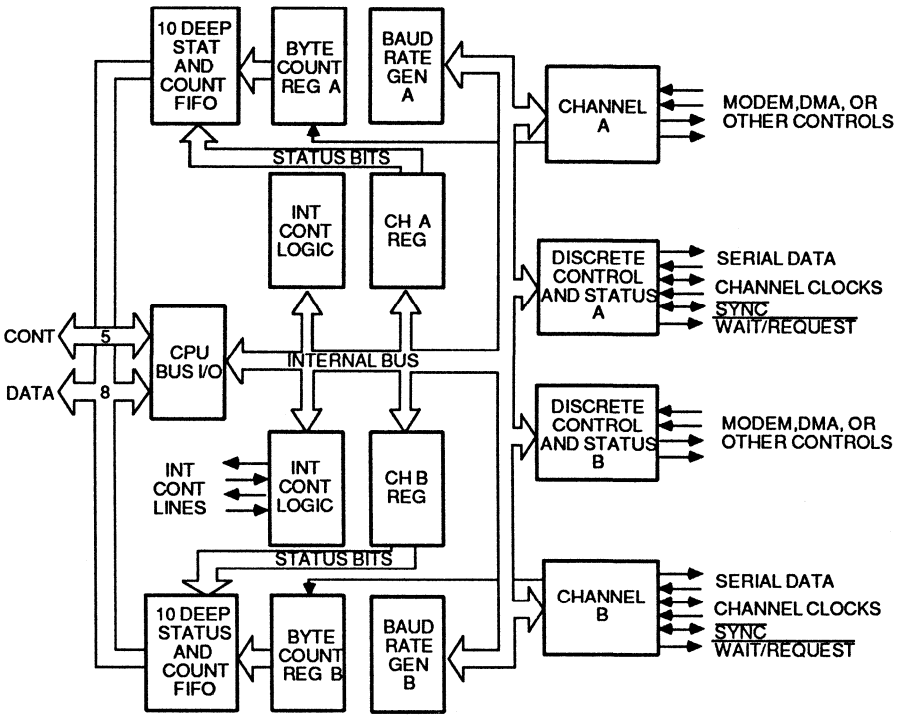
The ESCC handles asynchronous formats, such synchronous byte-oriented protocols as IBM Bisync and such synchronous bit-oriented protocols as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.), including DMA.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels, in addition to its Byte - Counting Register and FIFO in SDLC mode.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C35-10PC	10 MHz	Plastic DIP
VL85C35-10QC		Plastic Leaded Chip Carrier (PLCC)
VL85C35-10CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 7

TELECOM PRODUCTS

Catalog
Product
Descriptions

VL7C103

300 BPS MODEM

FEATURES

- Low-cost single-chip 300 bit-per-second (bps) modem
- Full answer and originate option
- Uses switched capacitor filters
- Implements all filters and hybrid circuits on-chip
- Output level up to -9 dBm with 600 Ω line impedance
- Analog loopback capability for testing
- Power-down mode for low-power use
- Low power consuming, single 5 V CMOS design
- Bell 103-compatible
- Direct replacement for the National Semiconductor NS74HC943 and Sierra Semiconductor SC11003
- Functional replacement for Texas Instruments TMS99532

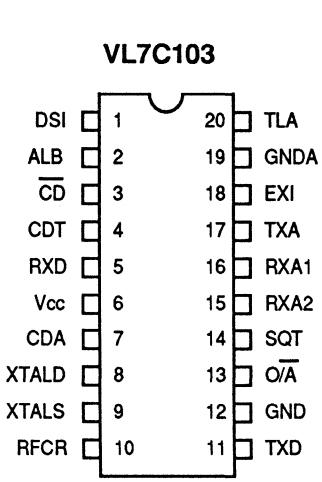
DESCRIPTION

The VL7C103 is a single-chip, full-duplex, 300 bit-per-second (bps) modem, compatible with the Bell 103 specifications. It is intended for data communications over general switched telephone networks, and can also be used with other voice-band channels.

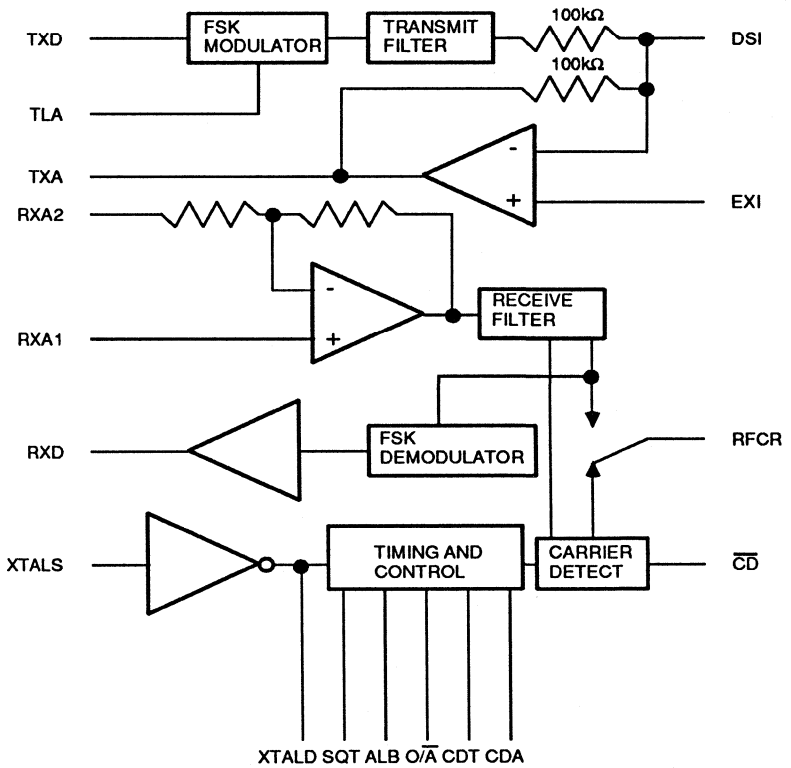
The VL7C103 requires a single 5 volt power supply, and is implemented in 3-micron switched-capacitor technology. This part is pin-for-pin compatible with the National Semiconductor NS74HC943, Sierra Semiconductor SC11003, and is functionally compatible with the Texas Instruments TMS99532.

Applications include integrated and stand-alone low-speed modems for terminals, personal computers, business systems, remote diagnostic systems, and business machines. Since the VL7C103 is a CMOS circuit, it is ideal for built-in modems in portable or lap-top computers.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C103-PC	Plastic DIP
VL7C103-CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL7C211

212A/V.22 MODEM FILTER

FEATURES

- Transmit-and-receive filter with half-channel compromise amplitude and group delay equalization
- Built-in call progress mode and answer / originate mode switching
- Bell 212A and CCITT V.22 compatible, with V.22 notch filters included
- Analog loopback capability for in-circuit testing
- Improved data transmission characteristics for lower bit error rate
- No external logic or multiplexers required
- Supports both North American and European modem designs

DESCRIPTION

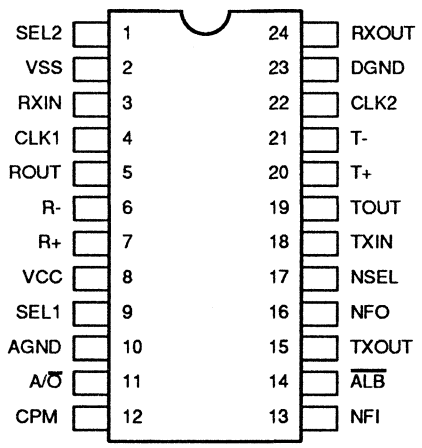
The VL7C211 modem filter is a monolithic CMOS switched-capacitor filter circuit designed for use in full-duplex 1200-bit-per-second modems. It meets the filtering requirements of the Bell 212A and CCITT V.22 modem specifications and includes high-band (2400 Hz) and low-band (1200 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, and smoothing filters for both bands. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. Also included in the VL7C211 filter are two uncommitted operational amplifiers that can be used for anti-aliasing filters or for gain control.

The VL7C211 is pin- and function-compatible with the Sierra SC11005, the AMI S35212 and S35212A. Further, the high-band filter in this filter can be scaled by a factor of six so that it can be used to monitor call progress tones in an intelligent modem. And, like the S35212A, it contains analog loopback so that the signal path can be completely tested.

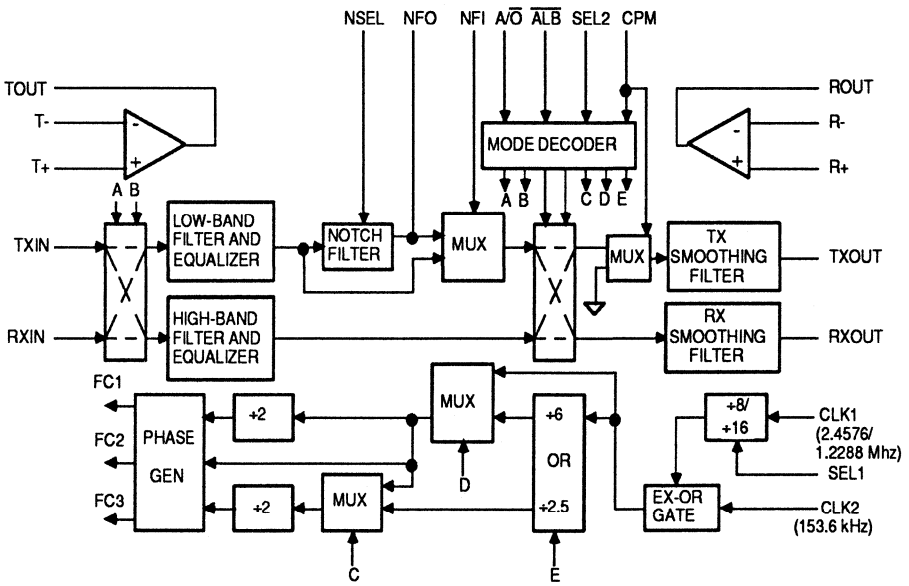
The VL7C211 offers enhanced call progress monitoring features. Besides being able to scale the high-band filter by a factor of six, the low-band filter can be scaled by a factor of 2.5 for better centering over the call progress frequency range of from 300 to 660 Hz. It also allows the unscaled high-band filter to be used for monitoring the modem answer tone, simplifying the design of full auto-dial / auto-answer modems.

PIN DIAGRAM

VL7C211



BLOCK DIAGRAM



Notes:

1. Pins 1, 4, 11, 12, 13, 17, and 22 have internal pull-down resistors to ground.
2. Pin 14 has an internal pull-up to VCC.

ORDER INFORMATION

Part Number	Package
VL7C211-PC	Plastic DIP
VL7C211-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL7C212A

300/1200 BIT-PER-SECOND MODEM

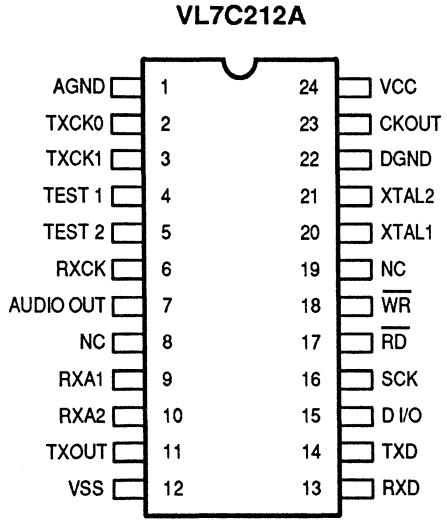
FEATURES

- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF and V.22 guard tones
- Bell 212A and CCITT V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital and remote digital loopback capabilities
- 24-pin DIP and 28-terminal plastic leaded chip carrier available
- High level of integration provides a highly cost-effective 300/1200 bit-per- second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11004

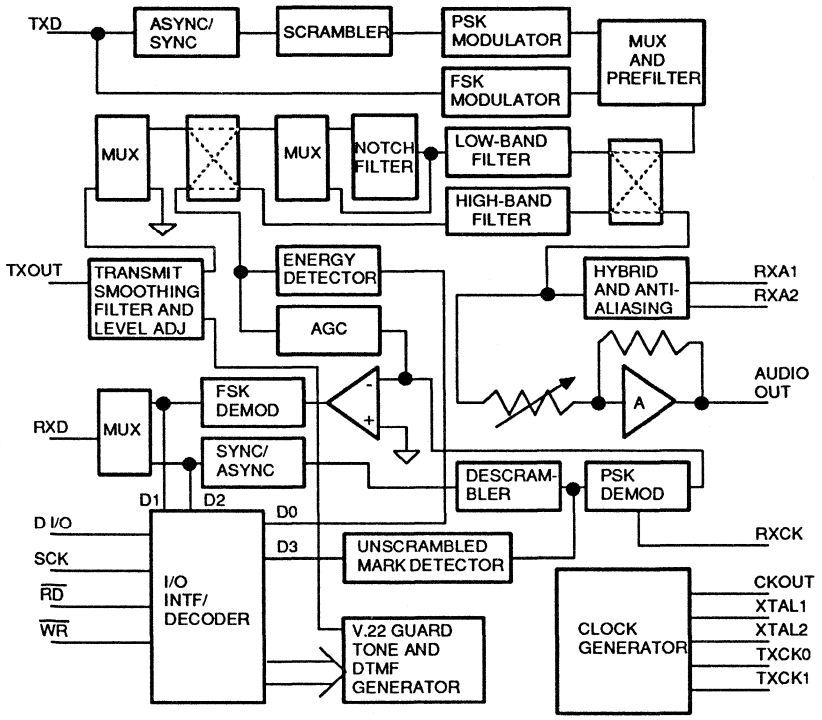
DESCRIPTION

The VL7C212A is a complete 300/1200 bit-per-second modem. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A or V.22 modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C212A also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C212A-PC	Plastic DIP
VL7C212A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL7C213

PARALLEL BUS MODEM CONTROLLER

FEATURES

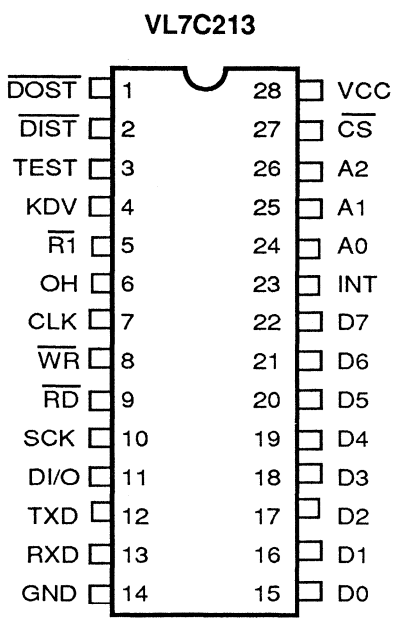
- Direct interface to VL7C212A single-chip modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- 2-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Direct replacement for Sierra SC11007
- Reduces board space and component count requirements

DESCRIPTION

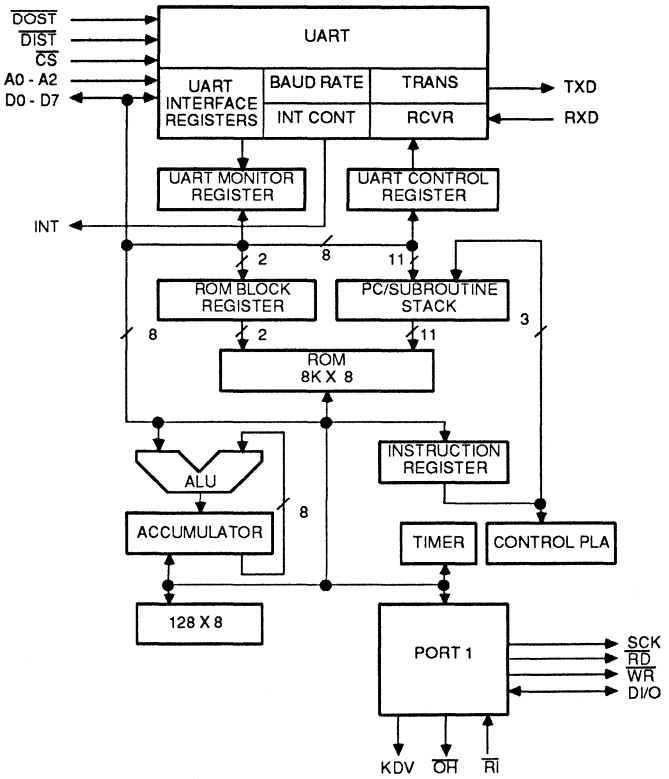
The VL7C213 Parallel Bus Modem Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C213 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C213 implements a Hayes-type smart modem for board-level, integral-modem applications.

Because the VL7C213 fully emulates the functions of the VL82C50 UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with the VL7C213/ VL7C212A chip set. In addition to including the functionality of the VL82C50 UART, the VL7C213 contains an 8-bit microprocessor, 8K by 8 bytes of ROM and 128 by 8 bytes of RAM.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C213-PC	Plastic DIP
VL7C213-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL7C214

STAND-ALONE MODEM INTERFACE CONTROLLER

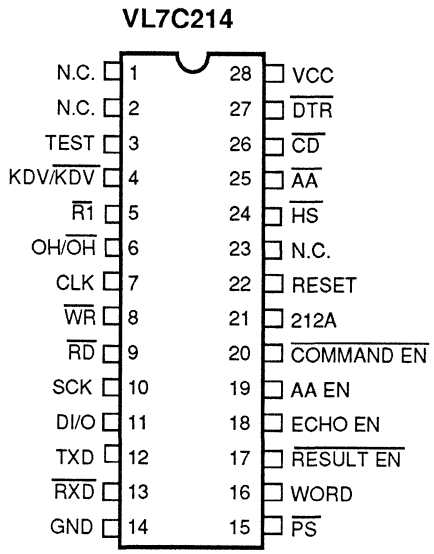
FEATURES

- Direct interface to VL7C212A single-chip modems
- Complete Hayes AT command set in firmware
- Built-in UART for RS232C interface
- 2-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry standard software
- Reduces board space and component count requirements
- Low power consumption
- Direct replacement for Sierra SC11008

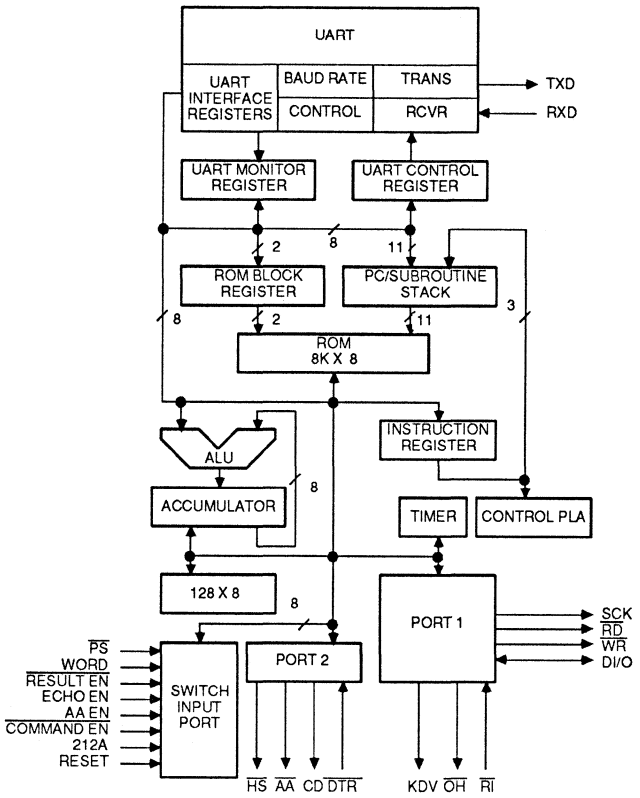
DESCRIPTION

The VL7C214 Stand-Alone Modem Interface Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C214 provides a highly cost-effective solution for interfacing a modem IC to a computer's RS232C port. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C214 implements a Hayes-type smart modem for stand-alone modem applications. All of the popular communications software written for the IBM PC will work with the VL7C214/VL7C212A chip set. The VL7C214 contains an 8-bit microprocessor, 8K by 8 bytes of ROM and 128 by 8 bytes of RAM. In order to support the stand-alone functionality of the device, an 8-bit switch input port allows immediate user access and manual control of the system. Either Bell 103 or CCITT V.22 may be selected in this manner.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C214-PC	Plastic DIP
VL7C214-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL80C75

T1 INTERFACE

FEATURES

- Supports T1, T1C and CEPT data rates
- AMI, B8ZS, HDB3 coding
- Meets AT&T Technical Advisory #34 for DSX1 and DSX1C interface standards
- Meets AT&T publication 43802 standard for jitter tolerance
- Meets AT&T jitter standard for digital channel bank
- Meets CCITT recommendation G.703 for 1.544 Mbps and 2.048 Mbps
- On-chip voltage comparators and AGC
- Input frequency memory
- Jitter-smoothing FIFO
- Loop control feedback
- Error detection and flagging
- Self-test provision
- Microprocessor-compatible interface
- Low-power CMOS technology

DESCRIPTION

The VL80C75 is a general-purpose PCM line interface circuit. It is designed to provide a bipolar interface according to T1 (1.544 Mbps), T1C (3.152 Mbps), or CEPT (2.048 Mbps) specifications. It is capable of sending (encoding) and receiving (decoding) AMI, B8ZS or HDB3 data formats.

The incorporation of on-chip voltage comparators and adaptive reference levels, allows the device decoder section to accept incoming ternary/bipolar data directly. Sensitivity is optimized by monitoring the level of the incoming bipolar signal.

An injection-locking divider permits clock recovery from the incoming serial data stream. A 32-bit-long FIFO (elastic buffer) may be used in either the decoder or the encoder path to smooth clock jitter. Status information is provided to facilitate the control of an external VCO.

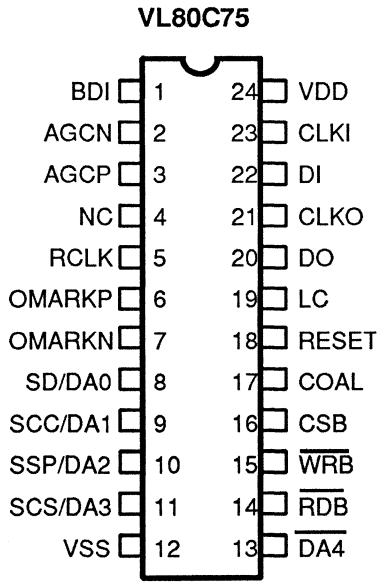
The VL80C75 indicates the presence of bipolar violations in the input data as well as a FIFO underflow/overflow.

Interfacing to the external bipolar line driver is facilitated by the provision of 50% duty cycle drive pulses. The system interface is microprocessor-compatible. The internal control registers may be accessed by either a serial or parallel interface.

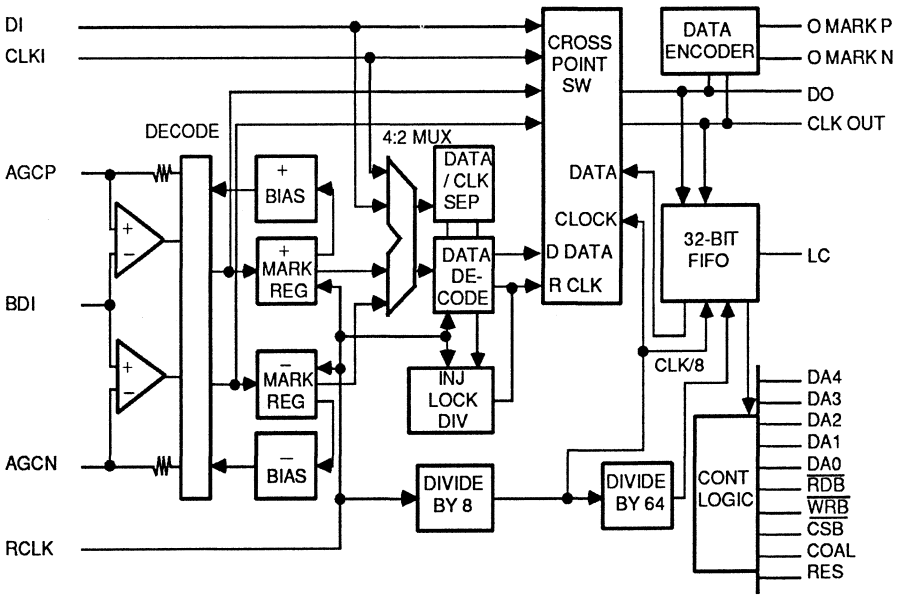
System test is assisted by the provision of a loopback feature that operates in both directions.

The VL80C75 is fabricated in a double-metal, n-well, 2-micron silicon-gate CMOS process and is housed in a 24-pin 300 mil DIP or ceramic package.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL80C75-PC	Plastic DIP
VL80C75-CC	Ceramic DIP
VL80C75-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 8

APPLICATION SPECIFIC MEMORY PRODUCTS DIVISION

Catalog
Product
Descriptions

APPLICATION SPECIFIC MEMORY PRODUCTS

GENERAL

The Application Specific Memory Products Division manufactures and markets application-specific and advanced memory products that directly address the high-performance requirements of applications at the leading edge of the electronics industry. It has a three-part strategy that calls for it to drive VLSI Technology's process technology, support the Corporation's overall ASIC strategy, and grow the Corporate revenues.

In pursuing its strategy, the Memory Products Division is concentrating on the development and manufacture of advanced memory products in four major areas: ROMs, EPROMs, SRAMs, and application-specific memories (ASMs), which are defined as memories that have the support logic required for system interface and control functions incorporated into the chip. In addition to offering its memories as catalog products, VLSI has also incorporated many of the advanced memory functions into its ASIC libraries as compiled cells, providing product technology that is required for ASIC design.

The Memory Products Division is located at:

1109 McKay Drive
San Jose, CA 95131
408/434-3000

ASMs (APPLICATION SPECIFIC MEMORIES)

Device	Function	Size	Organization	Access Time	Technology	Pins	Package	Available
VT2130	Dual-Port RAM	8K	1,024 x 8	100 ns	HMOS	48	Plastic	Now
VT2131	Dual-Port RAM	8K	1,024 x 8	100 ns	HMOS	48	Plastic	Now
VT16DP8	Dual-Port RAM	16K	2,048 x 8/1,024 x 16	60 ns	HCMOS	64	PLCC	Now
VT16AM8	Dual-Port RAM	16K	2,048 x 8/1,024 x 16	60 ns	HCMOS	52	PLCC	Now
VT1VF8	FIFO	10K	1,280 x 8	50 ns	HCMOS	28	Plastic	Q287
VT2F9	FIFO	18K	2,048 x 9	50 ns	HCMOS	28	Plastic	Q187
VT2F91	FIFO	18K	2,048 x 9	50 ns	HCMOS	44	PLCC	Q187
VT8K9	Parity RAM	72K	8,192 x 9	35 ns	HCMOS	28	Ceramic	Now
VT64R4	REGRAM	64K	16,384 x 4	40 ns	HCMOS	28	Plastic	Q287
VT7132	Dual-Port RAM	16K	2,048 x 4	55 ns	HCMOS	48	Plastic	Q287
VT7132A	Dual-Port RAM	16K	2,048 x 8	30 ns	HCMOS	48	Plastic	Q187
VT7142	Dual-Port RAM	16K	2,048 x 8	55 ns	HCMOS	48	Plastic	Q287
VT7142A	Dual-Port RAM	16K	2,048 x 8	30 ns	HCMOS	48	Plastic	Q187

SRAMs

Device	Function	Size	Organization	Access Time	Technology	Pins	Package	Available
VT7C122	SRAM	1K	256 x 4	15 ns	HCMOS	22	Plastic	Now
VT20C18	SRAM	16K	2,048 x 8	20 ns	HCMOS	24	Plastic	Now
VT20C68	SRAM	16K	4,096 x 4	20 ns	HCMOS	20	Plastic	Now
VT20C19	SRAM	16K	2,048 x 8	20 ns	HCMOS	24	Plastic	Now
VT20C69	SRAM	16K	4,096 x 4	20 ns	HCMOS	20	Plastic	Now
VT20C78	SRAM	16K	4,096 x 4	20 ns	HCMOS	22	Plastic	Now
VT20C79	SRAM	16K	4,096 x 4	20 ns	HCMOS	22	Plastic	Now
VT20C98	SRAM	64K	8,192 x 8	25 ns	HCMOS	28	Ceramic	Q287
VT20C99	SRAM	64K	8,192 x 8	25 ns	HCMOS	28	Ceramic	Q287
VT62KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	22	Plastic	Q287
VT63KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	24	Plastic	Q287
VT64KS4	SRAM	64K	16,384 x 4	35 ns	HCMOS	22	Ceramic	Now
VT64KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	22	Plastic	Q187
VT65KS4	SRAM	64K	16,384 x 4	35 ns	HCMOS	24	Ceramic	Now
VT65KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	24	Plastic	Q187
VT65KS4	SRAM	64K	16,384 x 4	35 ns	HCMOS	28	LCC	Now
VT66KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	28	Plastic	Q187
VT67KS4	SRAM	64K	16,384 x 4	25 ns	HCMOS	28	Plastic	Q187

HRAMs

Device	Function	Size	Organization	Access Time	Technology	Pins	Package	Available
VT64H1	RAM	64K	65,536 x 1	35 ns	HCMOS	24	Ceramic	Now
VT16H4	RAM	64K	16,384 x 4	35 ns	HCMOS	24	Ceramic	Now

ROMs

Device	Function	Size	Organization	Access Time	Technology	Pins	Package	Available
VT23512	ROM	512K	65,536 x 8	150 ns	HMOS	28	Plastic	Now
VT231024	ROM	1M	131,072 x 8	150 ns	HMOS	28	Plastic	Now

EPROMs

Device	Function	Size	Organization	Access Time	Technology	Pins	Package	Available
VT27C128	EPROM	128K	16,384 x 8	175 ns	HCMOS	28	Cerdip	Now
VT27C64	EPROM	64K	8,192 x 8	150 ns	HCMOS	28	Cerdip	Now
VT27C256	EPROM	256K	32,768 x 8	175 ns	HCMOS	28	Cerdip	Now
VT27C512	EPROM	512K	65,536 x 8	250 ns	HCMOS	28	Cerdip	Now

CERTIFIED EPROM PROGRAMMERS

DATA I/O (206/881-6444)

Programmer	VLSI Technology EPROM			
	VT27C64	VT27C128	VT27C256	VT27C512
DATA I/O	Rev 01	Note 1	Rev 01	Note 1
201	Note 1	Note 1	REV 01	Note 1
280	V02	Note 1	V01	Note 1
120A/121A	V10	V10	V10	V10
GANGPAK	Note 1	Note 1	Note 1	Note 1
UNIPAK	V07	V11	V07	V11
UNIPAK 2	V07	V11	V07	V11
UNIPAK 2B	V07	V11	V07	V11
Programming Voltage	12.5 V	12.5 V	12.5 V	12.5 V
Family/Pinout Code	5D/33, Note 2	5D/51, Note 2	5D/32, Note 2	4C/A4, Note 2
Alternatives	Note 3	93/51	93/32	

DIGILEC (201/493-2420)

Programmer		VLSI Technology EPROM
Model Number	Revision, Note 4	
803	B–7.0 B–1.0 Note 1	VT27C64, VT27C128 VT27C256 VT27C512
804	2.2 2.3 Note 1	VT27C64 VT27C128, VT27C256 VT27C512
824	1.1 1.4 2.0 Note 1	VT27C128 VT27C256 VT27C64 VT27C512
825	1.0 Note 1	VT27C64, VT27C128, VT27C256 VT27C512
828	A–1.0 A–2.1 Note 1	VT27C64, VT27C128 VT27C256 VT27C512

SUNRISE (818/914-1926)

Programmer		VLSI Technology EPROM
Model Number	Revision	
Z-1000B Universal Programmer	3.2	VT27C64, VT27C128, VT27C256, VT27C512
Z-1200	(Phasing out; not applicable)	
Z-3000	1.1	VT27C64, VT27C128, VT27C256, VT27C512
T816	1.0	VT27C64, VT27C128, VT27C256, VT27C512

Notes:
1. Still under development.
2. To be qualified by December 1986 (these family/pinout codes are the same as NSC).
3. Do not use the family/pinout code 35/33, as this requires a programming voltage of 21 V and can destroy the device.
4. Any revisions higher than those listed will incorporate VLSI EPROMs.

CERTIFIED EPROM PROGRAMMERS

EPRO (408/262-3912)

Programmer			VLSI Technology EPROM
Model Number	Revision	Callup Name	
EPRO 124 Gang Programmer	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 224 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 2000 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 2025 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 2028 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 2030 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512
EPRO 4000 System	815048990	VTI, Note 1	VT27C64, VT27C128, VT27C256, VT27C512

ELAN (415/964-5338)

Programmer			VLSI Technology EPROM
Model Number	Hardware Issue	Software Issue	
1200	1.01	P3.10	VT27C64, VT27C128, VT27C256, Note 2
1300	1.00	G3.10	VT27C64, VT27C128, VT27C256, Note 2
1012	1.01	P3.10	VT27C64, VT27C128, VT27C256, Note 2
C41	HW1	C1	VT27C64, VT27C128, VT27C256, Note 2
E2B	HW1	EB1	VT27C64, VT27C128, VT27C256, Note 2
E8B	HW1	EB1	VT27C64, VT27C128, VT27C256, Note 2
E9B	HW1	EB1	VT27C64, VT27C128, VT27C256, Note 2
E9C	HW1	EB1	VT27C64, VT27C128, VT27C256, Note 2
E12B	HW1	ESB1	VT27C64, VT27C128, VT27C256, Note 2
E16B	HW1	EB1	VT27C64, VT27C128, VT27C256, Note 2

STAG (408/745-1991)

Programmer				VLSI Technology EPROM
Model Number, Note 3	Module	Mainframe EPROM (2764)	Module EPROM (27512)	
PP39	39M100	Rev 5.3	Rev 15.0	VT27C64, VT27C128, VT27C256, VT27C512
PP40, Note 4	40M100	Rev 3.0	Rev 4.0	VT27C64, VT27C128, VT27C256, VT27C512
PP41, Note 4	41M100	Rev 2.0	Rev 3.0	VT27C64, VT27C128, VT27C256, VT27C512

Notes:

1. The callup name will change to VLSI by February 1987.
2. The ELAN device selection entries are "Intel 2764A" for the VT27C64, "Intel 27128A" for the VT27C128, and "Intel 27C256" for the VT27C256.
3. These programmers can be used immediately with the EPROM revisions listed. Stag will include EPROMs with new equipment orders.
4. The PP40 and PP41 are replacements for the PP16 and PP16A. They have the ability to program CMOS EPROMs, are expandable, and are approximately one-half the price.

CERTIFIED EPROM PROGRAMMERS

OLIVER ADVANCED ENGINEERING (201/493-2420)

Programmer		VLSI Technology EPROM
Model Number	OMNI Database Upgrade, Note 1	
OMNI 28	OM-E100, Rev 01	VT27C64, VT27C128, VT27C256
OMNI 40	OM-E100, Rev 01	VT27C64, VT27C128, VT27C256
OMNI 64	OM-E100, Rev 01	VT27C64, VT27C128, VT27C256

INTERNATIONAL MICROSYSTEMS INC. (408/245-7180)

Programmer Model Number	VLSI Technology EPROM
IM3016A, Note 2	Consult IMI factory

Notes:

1. Upgrades can be done through direct factory modem, floppy disk, or library module (for overseas travel).
2. This programmer must be sent to the IMI factory for an upgrade in order to program VLSI Technology devices. Without this upgrade, it will not program correctly. IMI will be producing a new programmer, the EPROM 1, that will be certified for VLSI Technology devices by the first quarter of 1987.

VLSI TECHNOLOGY, INC.

SECTION 9

RAM PRODUCTS

Catalog
Product
Descriptions

VLSI TECHNOLOGY, INC.

PRELIMINARY **VT16H4 • VT16H41**

16,384 x 4 HRAM™

FEATURES

- High-speed 35 ns read, write and cycle times
- Static Column—25 ns to 256 4-bit words
- Single clock timing—no precharge
- Active HIGH controls—low power
- Single 5 V (±10%) supply, 0°C to 70°C operation
- Low power (typ)—315 mW active, 0.3 mW standby
- Extended refresh—4 ms on 64 rows
- High-efficiency refresh, < 0.1% overhead loss
- Optimized pinout
- Mask level alternate-sourced by VISIC and MMI
- Common or separate data I/O pin-outs: V16H4—Common data I/O V16H41—Separate data I/O

DESCRIPTION

The VT16H4 and VT16H41 Hierarchical Random Access Memory (HRAM) offers a new cost-effective approach to achieving very fast access times while maintaining high bit density and low operating power. The 16,384-word by 1-bit memories are fabricated using an advanced 1.5-micron HCMOS process.

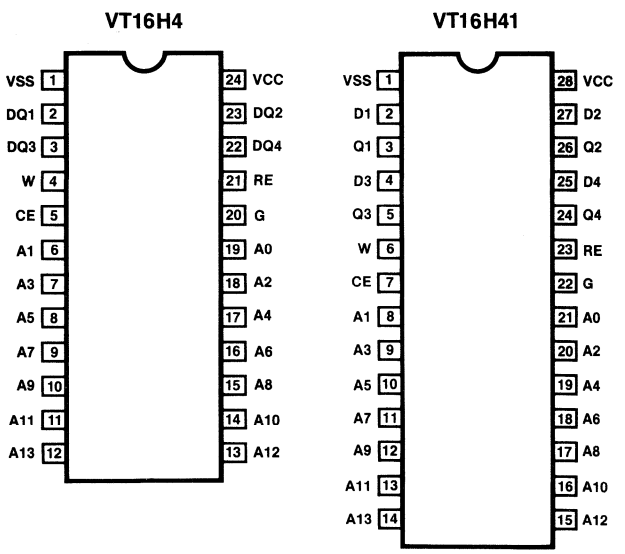
The HRAM architecture allows read, write and cycle times of 35 ns to any one of 16,384 bits of information contained in the memory. The static column mode allows a 25 ns read, write and cycle to any of 256 4-bit words defined by the column addresses.

Two package options are provided for greater system design flexibility. The 24-pin, 300-mil DIP VT16H4 with common data I/O pins offers higher board space efficiency, while the 28-pin, 400-mil DIP VT16H41 with separate data I/O pins allows higher system performance.

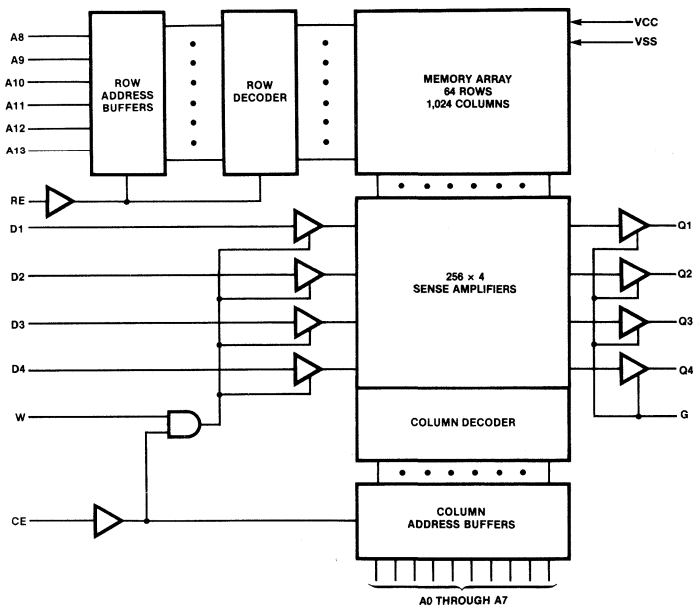
The VT16H4 and VT16H41 provide new standards of performance well beyond those available for static RAMs, without the associated power dissipation and cost penalties. With mask- and process-compatible alternate sources provided through technology exchange agreements with VISIC, Inc. (V64H1), the VT16H4 and VT16H41 offer new solutions for the expanding demand for high-performance CMOS memories.

™ HRAM is a trademark of VISIC, Inc.

PIN CONFIGURATION



BLOCK DIAGRAM



NOTE: VT16H4—inputs and output internally connected.

PIN NAMES

A0-A7	Column Address
A8-A13	Row Address
RE	Row Enable
W	Write Enable
G	Output Enable

CE	Column Enable
DQ1-DQ4 (VT64H4)	Data Inputs/Outputs
VCC	Power (5 V)

VSS	Ground (0 V)
D1-D4 (VT64H41)	Data Inputs
Q1-Q4 (VT64H41)	Data Outputs

VT20C18 • VT20C19

2,048 × 8 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C19)
- Automatic power-down when deselected (VT20C18)
- CMOS process for low power:
  - 550 mW (typical) active
  - 35 mW (typical) standby (VT20C18)
  - 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- All pins capable of withstanding electrostatic discharge greater than 2000 V
- 300-mil, 24-pin dual in-line package

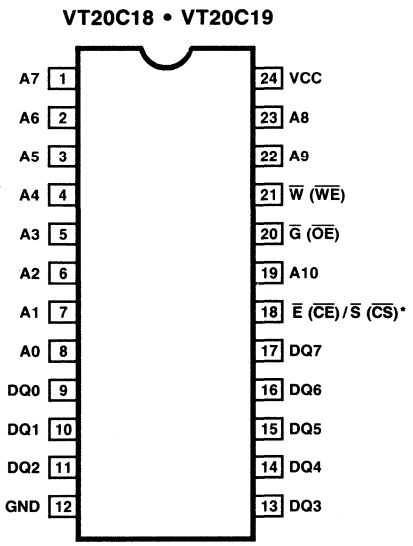
DESCRIPTION

The VT20C18 and VT20C19 are high-speed static RAMs (SRAMs) that are organized as 2,048 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power, making them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

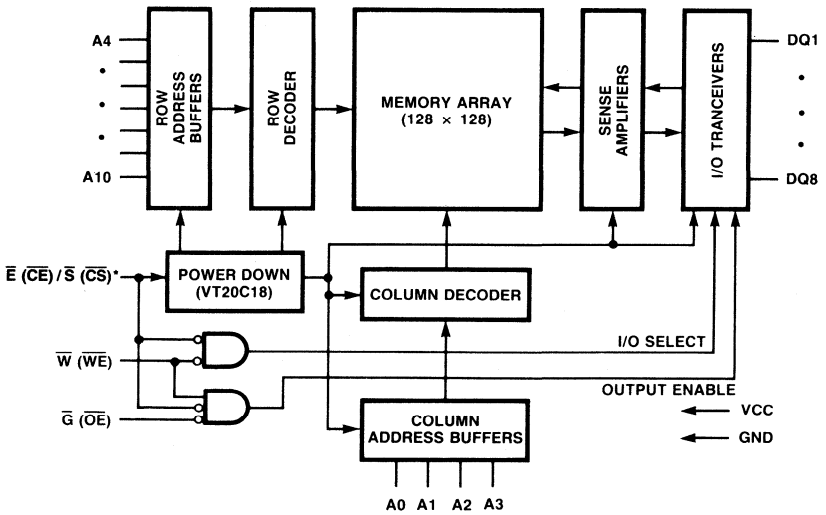
The VT20C18, with automatic power-down, offers standby current of only 7 mA when deselected. The VT20C19 offers a fast chip select option that provides data access in only 12 ns.

For easy memory expansion, both devices have active-low chip enable ($\overline{E}$), output enable ($\overline{G}$) and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C18 and VT20C19 are packaged in 300-mil DIPs with industry-standard pinouts, but offer higher speeds for increased system performance.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A10	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C19 only.

VT20C68 • VT20C69

4,096 × 4 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, 35 and 45 ns
- Fast chip select option: 12, 15, 20 and 25 ns (VT20C69)
- Automatic power-down when deselected (VT20C68)
- CMOS process for low power:
  - 550 mW (typical) active
  - 35 mW (typical) standby (VT20C68)
  - 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2000 V
- 300-mil, 20-pin dual in-line package
- Pin-compatible with standard 4K × 4 SRAMs

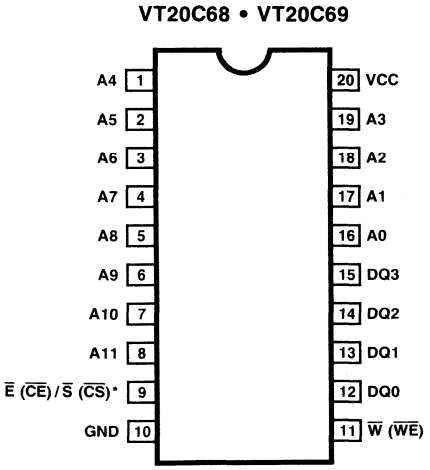
DESCRIPTION

The VT20C68 and VT20C69 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

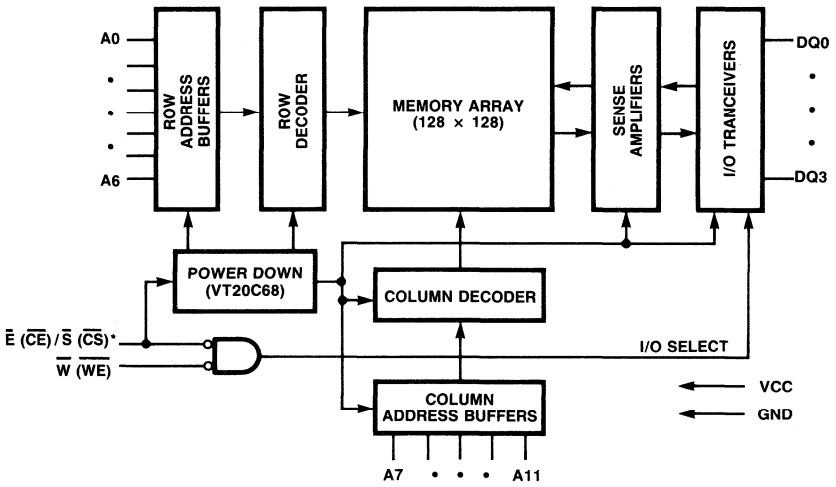
The VT20C68, with automatic power-down, offers standby current of only 7 mA when deselected. The VT20C69 offers a fast chip select option that provides data access in only 12 ns.

For easy memory expansion, both devices have active-low chip enable ($\overline{E}$) and write enable ($\overline{W}$) signals as well as three-state outputs. The VT20C68 and VT20C69 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Inputs
DQ0–DQ3	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C69 only.

VT20C78 • VT20C79

4,096 × 4 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, 35 and 45 ns
- Fast output enable control
- Fast chip select option: 12, 15, 20 and 25 ns (VT20C79)
- Automatic power-down when deselected (VT20C78)
- CMOS process for low power:
  - 550 mW (typical) active
  - 35 mW (typical) standby (VT20C78)
  - 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2000 V
- 300-mil, 22-pin dual in-line package
- Pin-compatible with standard 4K x 4 SRAMs

DESCRIPTION

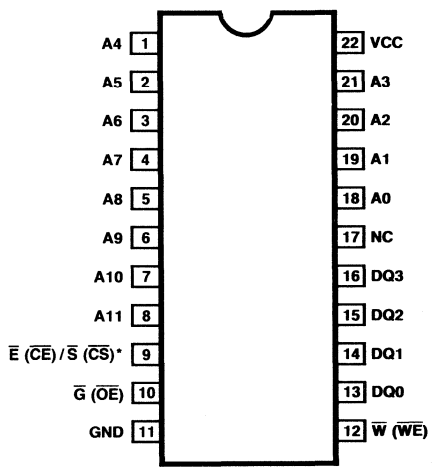
The VT20C78 and VT20C79 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C78, with automatic power-down, offers standby current of only 7 mA when deselected. The VT20C79 offers a fast chip select option that provides data access in only 12 ns.

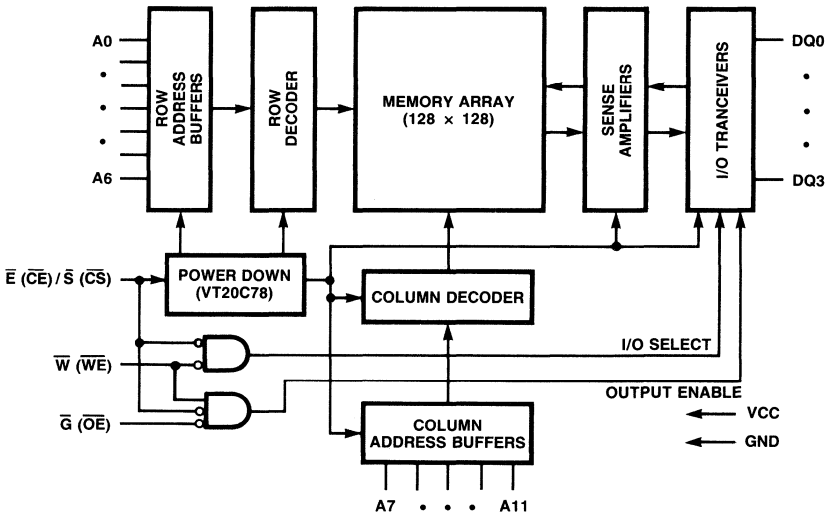
For easy memory expansion, both devices have active-low chip enable ($\overline{E}$), output enable ($\overline{G}$), and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C78 and VT20C79 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

PIN DIAGRAM

VT20C78 • VT20C79



BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Inputs
DQ0–DQ3	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$) / $\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C79 only.

PRELIMINARY

VT20C98 • VT20C99

8,192 × 8 SRAM

FEATURES

- High-speed access and cycle times: 25, 35 and 45 ns
- Fast chip select option: 15, 20 and 25 ns (VT20C99)
- Automatic power-down when deselected (VT20C98)
- CMOS process for low power:
  - 550 mW (typical) active
  - 35 mW (typical) standby (VT20C98)
  - 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2001 V
- 300-mil, 28-pin dual in-line package
- Pin-compatible with standard 8K x 8 SRAMs

DESCRIPTION

The VT20C98 and VT20C99 are high-speed static RAMs (SRAMs) that are organized as 8,192 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

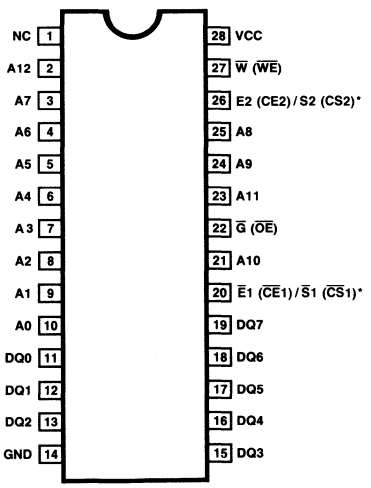
The VT20C98, with automatic power-down, offers standby current of only 20 μA when deselected. The VT20C99 offers a fast chip select option that provides data access in only 15 ns.

For easy memory expansion, both devices have active-low chip enable ($\overline{E}$), output enable ($\overline{G}$), and write enable ($\overline{W}$) signals, as well as three-state outputs. Both of the two chip enable inputs ($\overline{E}$1 and E2) must be used to activate the SRAM.

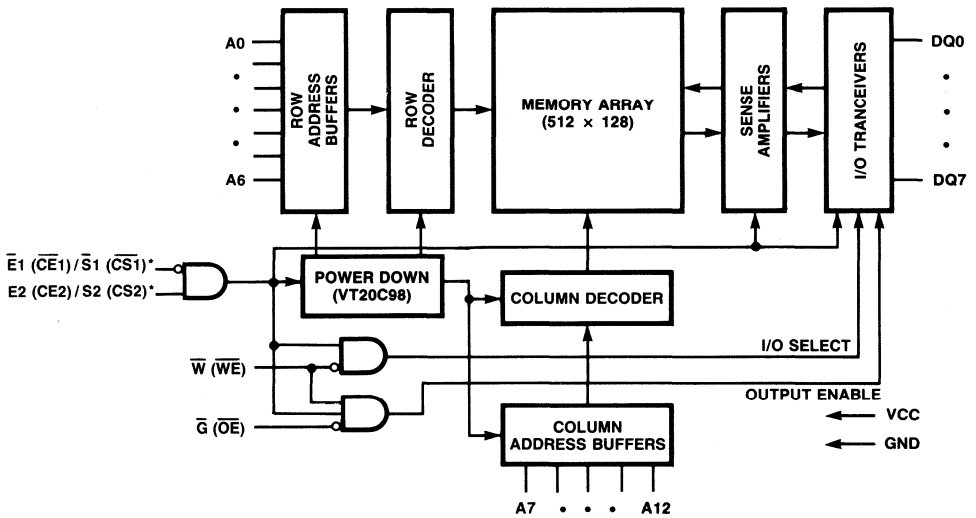
The VT20C98 and VT20C99 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

PIN DIAGRAM

VT20C98 • VT20C99



BLOCK DIAGRAM



PIN NAMES

A0–A12	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{E}$1 ($\overline{CE}$1)/$\overline{S}$1 ($\overline{CS}$1)* E2 (CE2)/S2 (CS2)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C99 only.

PRELIMINARY **VT64H1**

65,536 × 1 HRAM

FEATURES

- High speed 35 ns read, write, and cycle times
- Static Column—25 ns to 1,024 bits
- SNAP™ read cycle of 10 ns, 4-bits
- Single clock timing—no precharge
- Active HIGH controls—low power
- Single 5 V (±10%) supply, 0 to 70°C operation
- Low power (typ)—315 mW active, 0.3 mW standby
- Extended refresh—4 ms on 64 rows
- High efficiency refresh, < 0.1% overhead loss
- Optimized pinout
- High density 300 mil DIP

DESCRIPTION

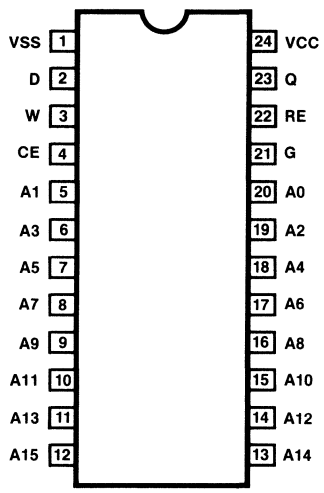
The VT64H1 HRAM* (Hierarchical Random Access Memory) offers a new cost effective approach to achieving very fast access times, while maintaining high bit density and low operating power. The 65,536 word by 1-bit memory is fabricated using an advanced 1.5-micron HCMOS process.

The HRAM architecture allows read, write and cycle times of 35 ns to any one of 65,536 bits of information contained in the memory. The static column mode allows a 25 ns read, write and cycle to any of the 1,024 bits defined by the column addresses. SNAP mode (Static Nibble Access Path), a third level of access, provides a random read access cycle of 10 ns to the four bits contained in the static column defined by addresses A0 and A1.

The VT64H1 provides new standards of performance well beyond those available for static RAMS, without the associated power dissipation and cost penalties. With mask and process compatible alternate sources provided through technology exchange agreements with VISIC, Inc. (V64H1) the VT64H1 offers new solutions for the expanding demand for high performance CMOS memories.

PIN CONFIGURATION

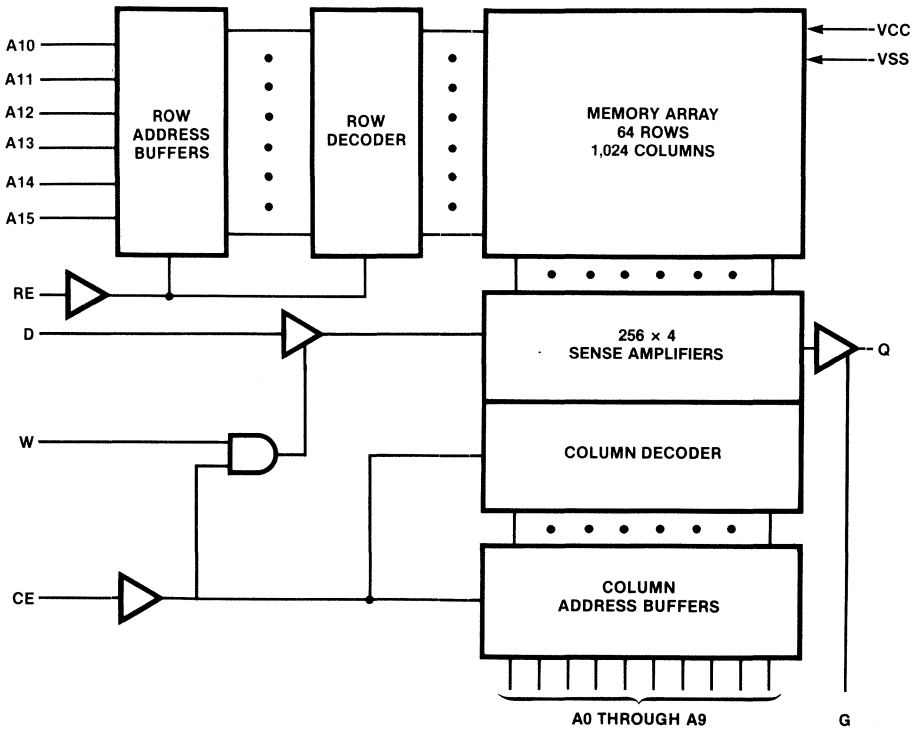
VT64H1



PIN NAMES

A0-A9	Column Address
A10-A15	Row Address
RE	Row Enable
W	Write Enable
G	Output Enable
CE	Column Enable
D	Data Input
Q	Data Output
VCC	Power (−5 V)
VSS	Ground (0 V)

BLOCK DIAGRAM



*HRAM™ and SNAP™ are trademarks of VISIC, Inc.

VLSI TECHNOLOGY, INC.

PRELIMINARY **VT64KS4•VT65KS4**

16,384 x 4 HIGH-SPEED 64K STATIC RAM

FEATURES

- 16,384 x 4-bit organization
- High-speed access time
  —25 ns max
- Low current
  —Operating: 100 mA max
  —Standby: 20 mA max
- Total static operation
- Single 5 V supply
- Output enable function (VT65KS4)
- Complete TTL compatibility
- 3-state I/O
- 22- and 24-pin JEDEC-approved pinout

DESCRIPTION

The VT64KS4 is a 64K high-speed static random access memory that is organized as 16,384 words by four bits.

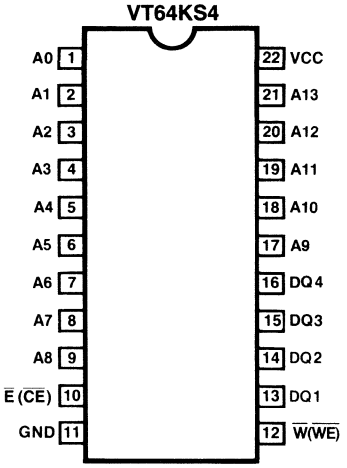
The device is fabricated in CMOS technology and achieves access times of 25 ns with a maximum power consumption of 500 mW. The high speed of the VT64KS4 enables it to replace bipolar and fast NMOS memories in many applications.

The fully static circuit requires no clocks or refreshing for operation. The VT64KS4 provides equal access and cycle times for ease of use. The output enable function of the VT65KS4 eliminates any potential bus contention.

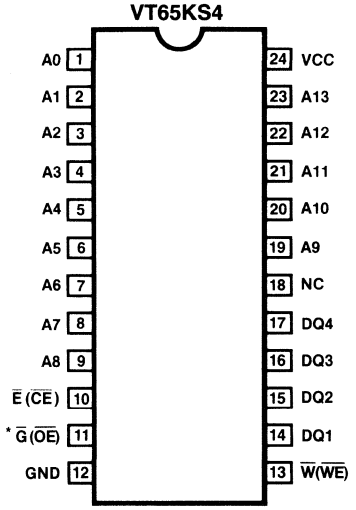
The device operates from a single 5 V power supply and is completely TTL compatible.

PIN DIAGRAMS

VT64KS4



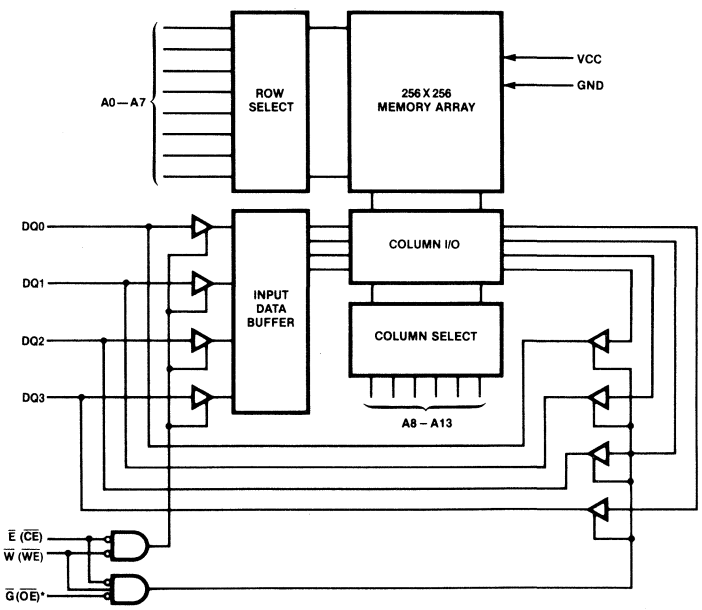
VT65KS4



PIN DESCRIPTIONS

A0 - A13	Address
DQ0 - DQ3	Data Input/Output
Ē(CE)	Chip Enable
*Ḡ (OE)	Output Enable
W̄(WE)	Write Enable
VCC	Power
GND	Ground

BLOCK DIAGRAM



*VT65KS4 ONLY

VT7C122

256 × 4 STATIC RAM

FEATURES

- High-speed access and cycle times: 15 ns
- CMOS process for low power: 330 mW (typical)
- Separate, TTL-compatible inputs and outputs
- All pins capable of withstanding electrostatic discharge greater than 2000 V.
- Industry-standard 22-pin dual in-line package

DESCRIPTION

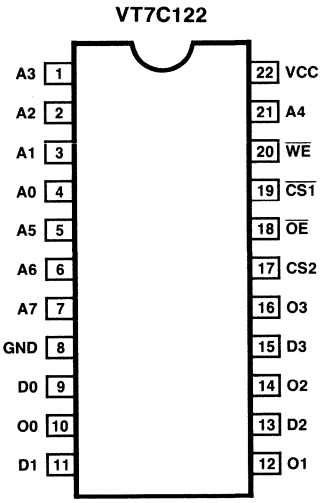
The VT7C122 is a high-speed static RAM (SRAM) that is organized as 256 words by 4 bits. If offers very high performance and reliability, as well as low power, making it ideally suited for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

For easy memory expansion, the VT7C122 has an active-LOW chip select one ($\overline{CS1}$) input, an active-HIGH chip select two (CS2) input, and three-state outputs.

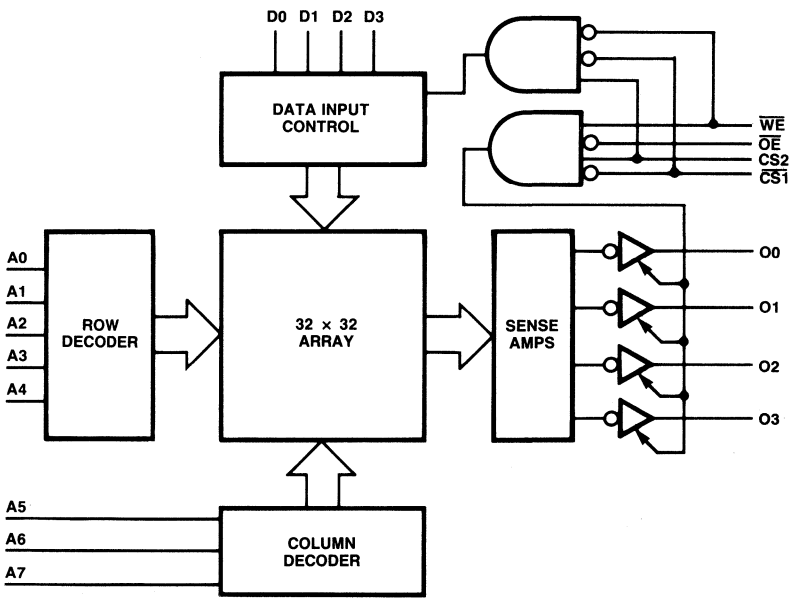
The read and write operations of the VT7C122 are controlled by an active-LOW write enable ($\overline{WE}$) input. When $\overline{WE}$ and chip select 1 ($\overline{CS1}$) are LOW and the chip select two (CS2) input is HIGH, information on the data input lines (D0 through D3) is written into the memory word addressed by the A0 through A7 inputs. Simultaneously, the output circuitry is preconditioned so that the correct data is available at the non-inverting output lines (O0 through O3) when the write cycle is complete. Preconditioning minimizes write recovery time by eliminating the "write recovery glitch."

To read data from the VT7C122, the $\overline{CS1}$ and output enable ($\overline{OE}$) inputs must be LOW while CS2 and $\overline{WE}$ are HIGH. The data stored in the addressed memory word is then read out on O0 through O3. These outputs go to an active-high-impedance state when $\overline{CS1}$ or $\overline{OE}$ is HIGH, CS2 is LOW, or when $\overline{WE}$ is LOW during the write operation.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A7	Address Inputs
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
D0–D3	Data Inputs
GND	Ground (0 V)
O0–O3	Data Outputs
$\overline{OE}$	Output Enable
VCC	Power (5 V)
$\overline{WE}$	Write Enable

VLSI TECHNOLOGY, INC.

SECTION 10

ASM PRODUCTS

Catalog
Product
Descriptions

PRELIMINARY **VT16AM8**

1K × 16, 2K × 8 DUAL-PORT RAM

FEATURES

- Organization
  - — Left Port: 1,024 × 16
  - — Right Port: 2,048 ×8
- High speed:
  - — 60 ns access
- Address/data 8-bit bus
- Fully static operation
- Full contention arbitration
- Simple microprocessor interface
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power:
  - — 60 mA (max) operating
- 52-pin PLCC

DESCRIPTION

The VT16AM8 is a 16,384-bit dual-port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. The right port has been organized with an address/data multiplexed bus to allow easy interfacing with most of the standard processors. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

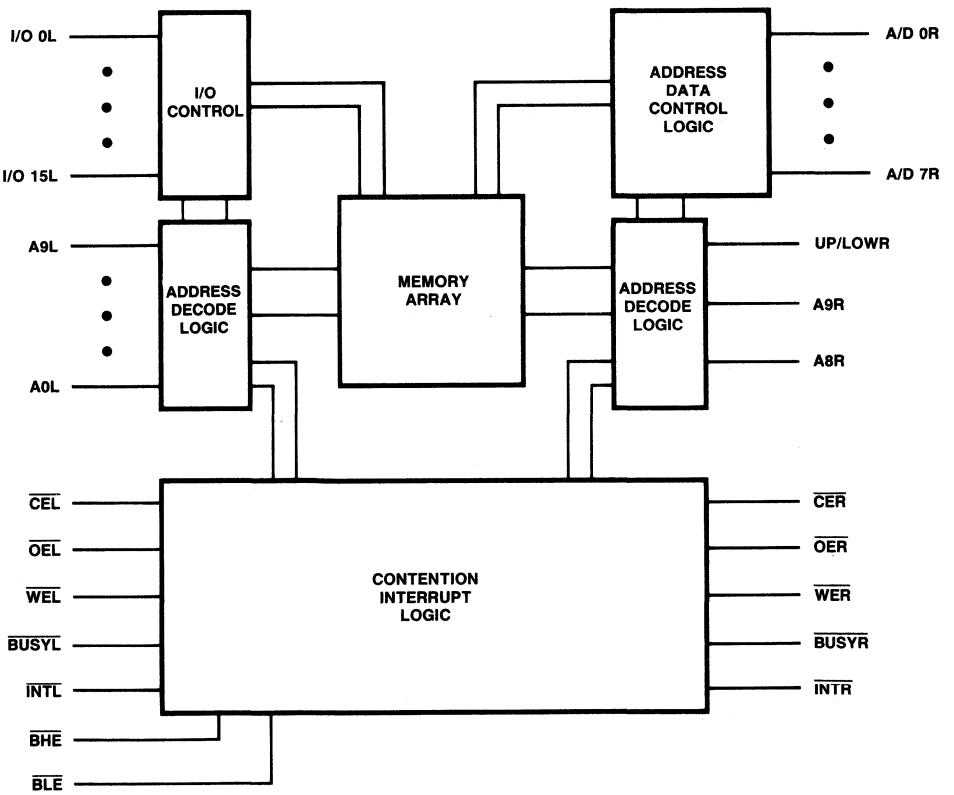
The VT16AM8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided. One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both control lines are active, the word mode is invoked.

Busy flags are open-drain for simple wired-OR operation.

Automatic power-down for each port is controlled independently by their chip enable inputs.

BLOCK DIAGRAM



PRELIMINARY **VT16DP8**

1K x 16, 2K x 8 DUAL-PORT RAM

FEATURES

- Organization:
  - — Left port: 1,024 x 16
  - — Right port: 2,048 x 8
- High speed:
  - — 60 ns access (max)
- Fully static operation
- Full contention arbitration
- Simple microprocessor interface
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Two interrupt flags
- Low power:
  - — 70 mA (max) operating
- 64-pin DIP or 68-pin PLCC

DESCRIPTION

The VT16DP8 is a 16,384-bit dual-port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

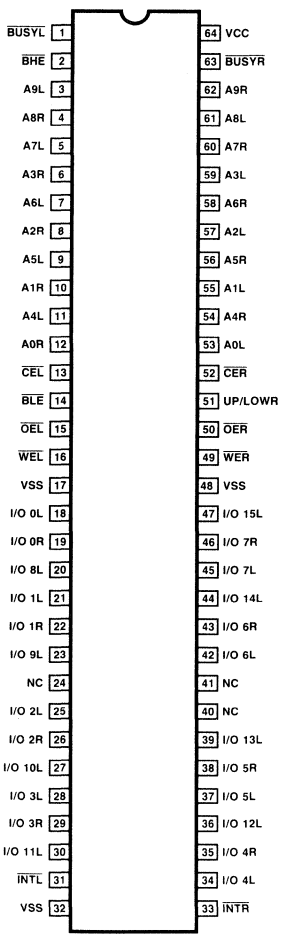
The VT16DP8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided.

One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

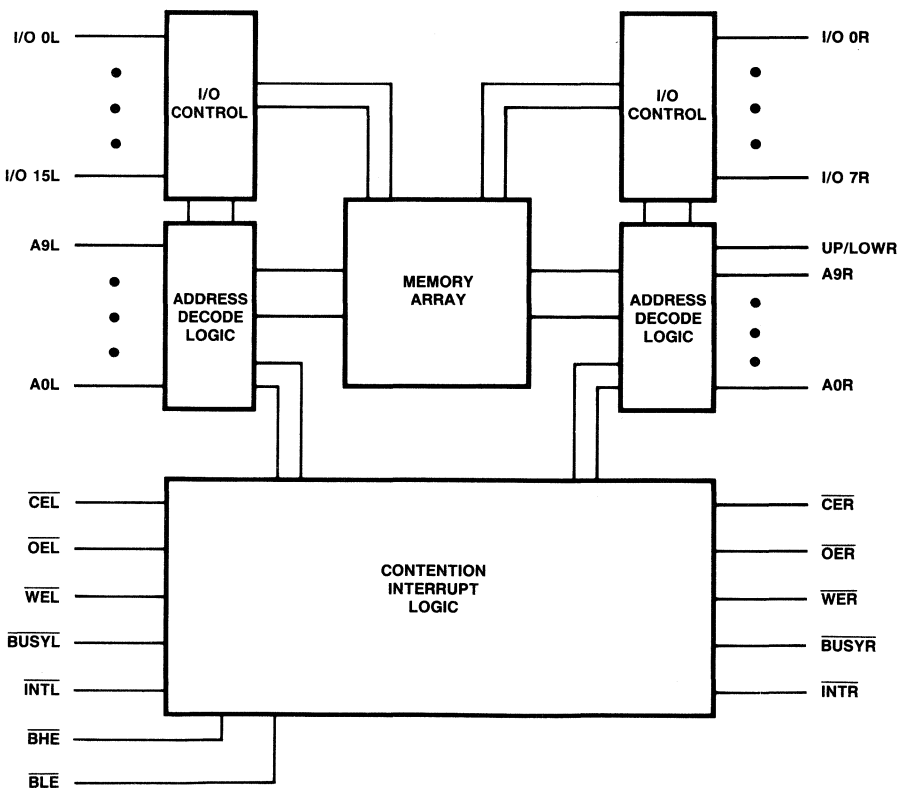
The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively.

PIN DIAGRAMS

VT16DP8



BLOCK DIAGRAM



1,024 x 8 DUAL PORT RANDOM ACCESS MEMORY

FEATURES

- 100 ns address access time
- Fully static operation
- Fully TTL Compatible
- Interrupt function ($\overline{INT}$): open drain for OR-tied operation
- Easy microprocessor interface
- VT2130—Transparent power down ($\overline{CE}$)
- VT2131—Non-power down ($\overline{CS}$)
- Output Enable function ($\overline{OE}$)
- Both ports operate independently
- Each port accesses entire memory
- $\overline{BUSY}$ function to handle contention

DESCRIPTION

The VT2130 and VT2131 are 8,192-bit Dual Port Static Random Access Memories organized 1,024 words by eight bits. They are designed using fully static circuitry and fabricated using n-channel double-poly silicon gate technology.

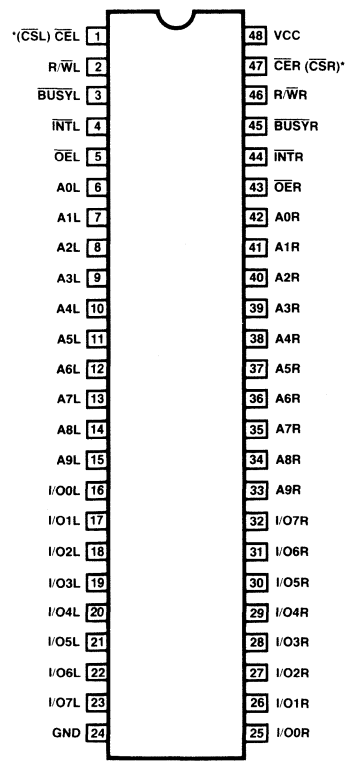
The VT2130 and VT2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The only situation where contention occurs is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side where the operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

An interrupt function ($\overline{INT}$) is provided to allow communication between systems. This function acts like a writable flag. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. The $\overline{INT}$s have open drain drivers to allow OR-tied operation.

The VT 2130 has an automatic power down feature which is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode.

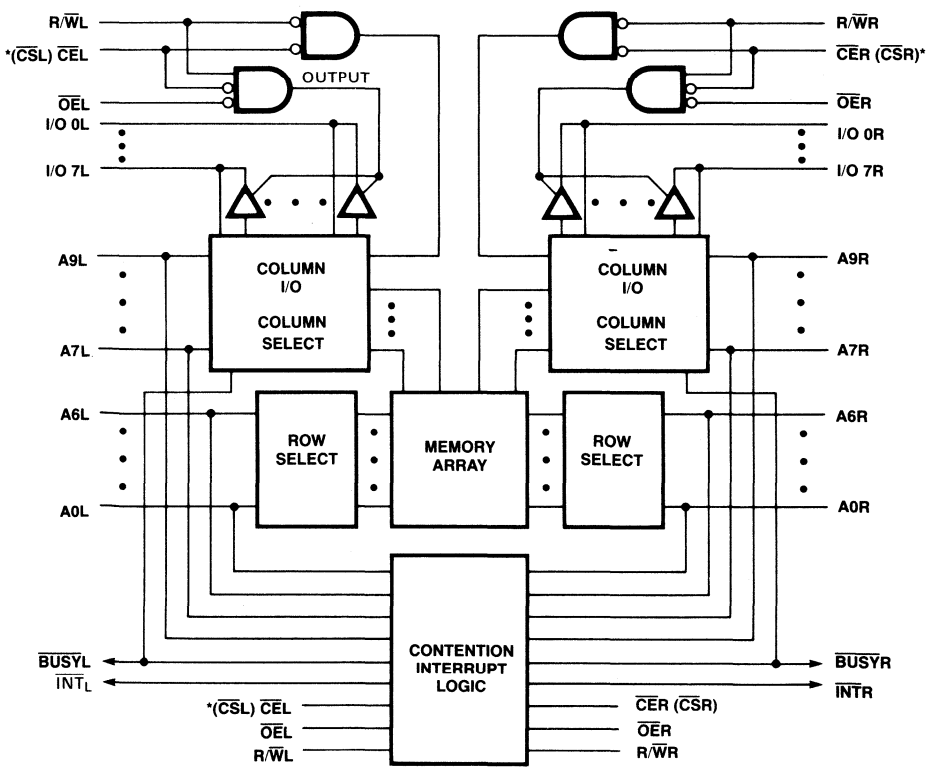
The VT2131 chip select (no power down) access has been designed to be faster than its address access so that the chip select decode time will not add to the memory's overall access time. This feature significantly improves system performance.

PIN CONFIGURATION



*SYMBOL IN (PARENTHESES) APPLIES TO VT2131

BLOCK DIAGRAM



PRELIMINARY **VT7132 • VT7142**

2K × 8 CMOS DUAL-PORT RAM

FEATURES

- High speed:
  — 55, 70, and 90 ns access
- Fully static operation
- Full contention arbitration
- VT7142 slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Dual interrupt flags in PLCC
- Low power:
  — 60 mA (max) operating
- 48-pin DIP or 52-pin PLCC

DESCRIPTION

The VT7132 and VT7142 are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "master" dual-port RAM with the VT7142 "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

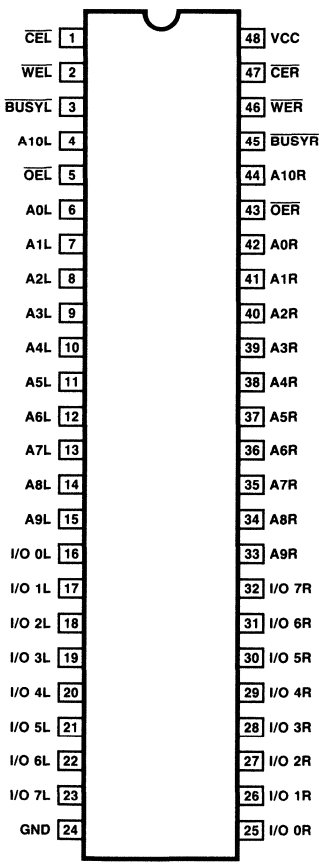
The VT7132/VT7142 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the left port takes priority.

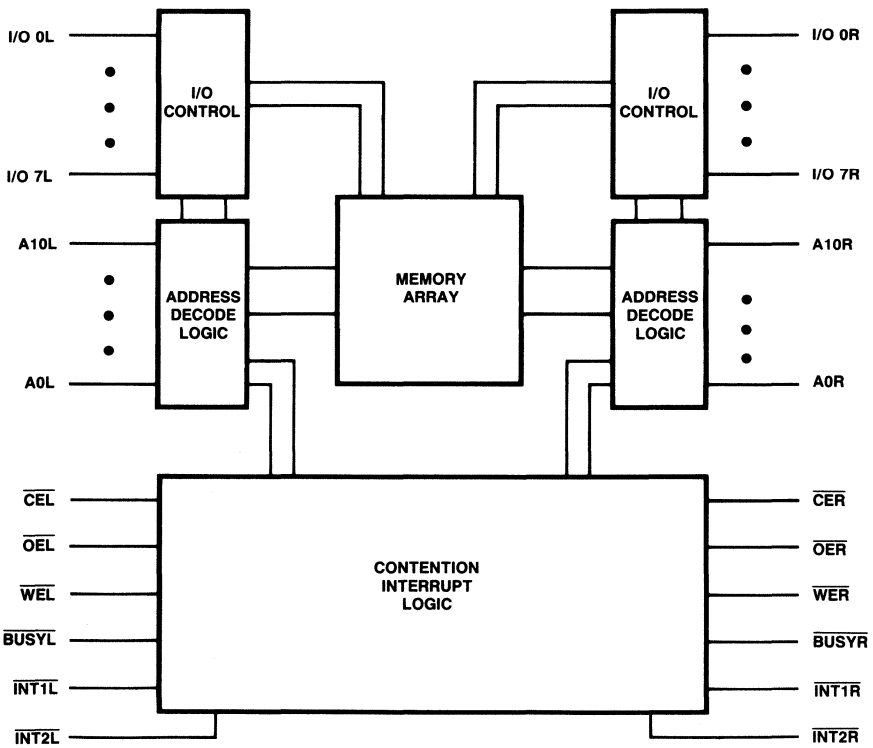
When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location is written from one side, the other side's INT pin goes low until the flag location is read by that side.

PIN DIAGRAM

VT7132 • VT7142



BLOCK DIAGRAM



PRELIMINARY **VT7132A • VT7142A**

HIGH-SPEED 2K × 8 CMOS DUAL-PORT RAM

FEATURES

- High speed:
  — 30, 35, and 45 ns access
- Fully static operation
- Full contention arbitration
- VT7142A slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Dual interrupt flags in PLCC
- Low power:
  — 60 mA (max) operating
- 48-pin DIP or 52-pin PLCC

DESCRIPTION

The VT7132A and VT7142A are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132A is designed to be used as a stand-alone 8-bit dual-port RAM or as a "master" dual-port RAM with the VT7142A "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

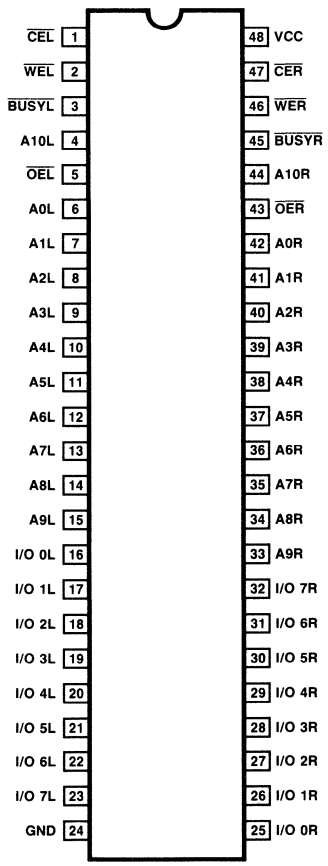
The VT7132A/VT7142A feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the left port takes priority.

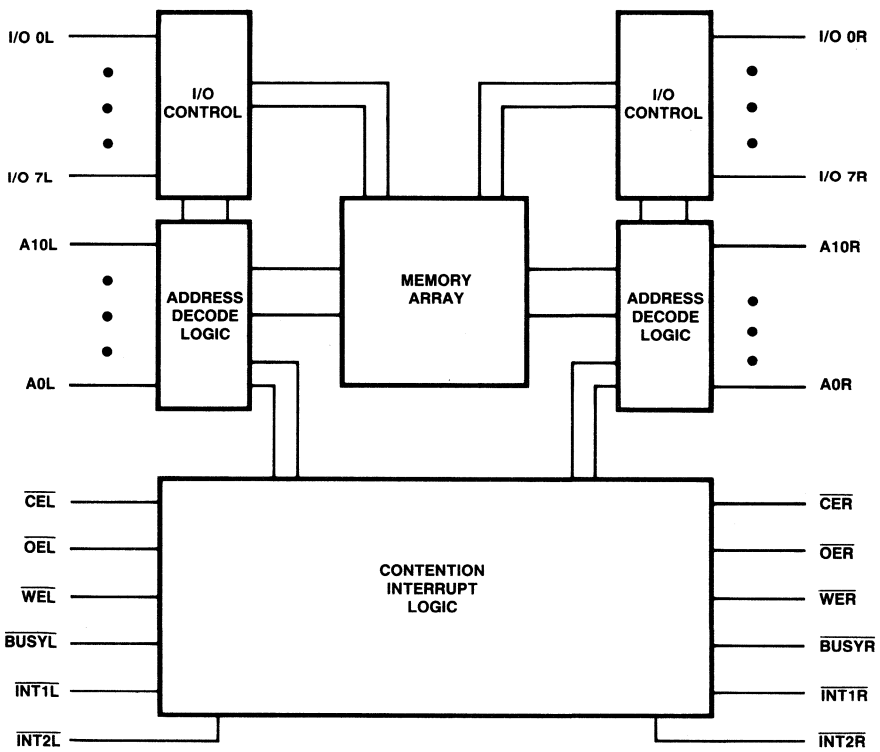
When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location is written from one side, the other side's INT pin goes low until the flag location is read by that side.

PIN DIAGRAM

VT7132A • VT7142A



BLOCK DIAGRAM



PRELIMINARY **VT8K9**

8,192 x 9 RAM

FEATURES

- High-speed 35 ns read, write, and cycle times
- Selectable on-chip parity bit generation/checking
- Single clock timing—no precharge
- Active HIGH controls—low power
- Single 5 V (±10%) supply, 0°C to 70°C operation
- Low power—500 mW active, 0.3 mW standby (typical)
- Extended refresh—4 ms on 64 rows
- Highly efficient refresh—less than 0.1% overhead loss
- Standard 400-mil-wide 28-pin side-brazed DIP
- Low noise—in-package decoupling capacitor

DESCRIPTION

The VT8K9 offers a new cost-effective approach to achieving very fast access times, while maintaining high bit density and low operating power. The 8,192-word by 9-bit memory is fabricated using an advanced 1.5-micron HCMOS process.

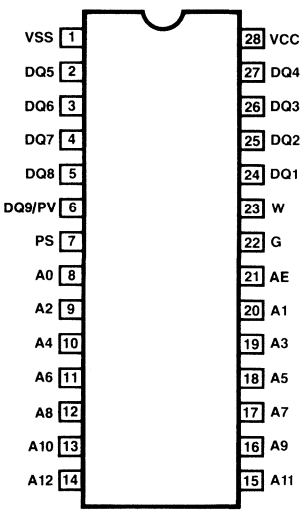
A parity select pin, PS, can configure the memory to nine bits of data or eight bits of data plus parity. The parity bit may be generated, stored and checked on-chip with minimum speed penalty. Parity may also be read from the chip into the system via the DQ9/PV pin.

To further ease system design, a novel technique eliminates the need for a pc board decoupling capacitor by providing a 0.2 μF decoupling capacitor on the 28-pin package used for the VT8K9 in order to reduce power line current spikes associated with multiple output devices.

The VT8K9 provides a unique combination of performance and low power beyond that available for high-performance static RAMs, along with a built-in parity generator/checker that significantly reduces the time required for parity compared to alternative methods. The VT8K9 offers new solutions for the expanding demand for high-performance CMOS memories.

PIN CONFIGURATION

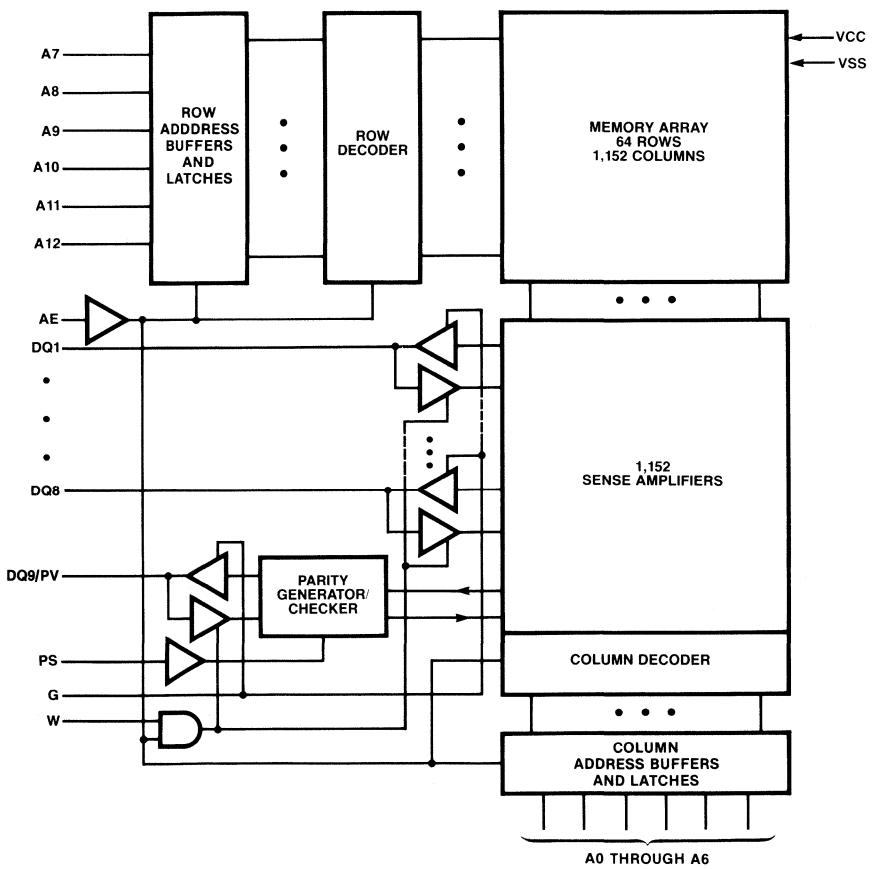
VT8K9



PIN NAMES

A0-A6	Column Address
A7-A12	Row Address
AE	Address Enable
W	Write Enable
G	Output Enable
PS	Parity Select
DQ1-DQ8	Data Inputs/Outputs
DQ9/PV	Data I/O / Parity Bit Verify
VCC	Power (+5 V)
VSS	Ground (0 V)

BLOCK DIAGRAM



VLSI TECHNOLOGY, INC.

SECTION 11

EPROM PRODUCTS

Catalog
Product
Descriptions

VT27C128

16,384 x 8 STATIC CMOS EPROM

FEATURES

- 16,384 x 8-bit organization
- Current— Operating: 15 mA max
  — Standby: 1.5 mA max
- Totally static operation
- Automatic power-down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC-approved pinout
- Programming—Voltage: 12.5 V
  —Current: 30 mA

DESCRIPTION

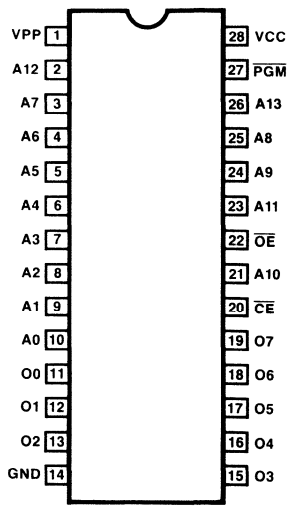
The VT27C128 is a 128K-bit high-performance CMOS erasable programmable read only memory that is organized as 16,384 bytes. It is compatible with all microprocessors and similar high-performance applications where high-density storage reprogrammability and simple interfacing are important design considerations.

The VT27C128 has automatic power-down that is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers-down and remains in a low-power standby mode. This unique feature provides substantial systems-level power savings. Another function of the VT27C128 is the Output Enable ($\overline{OE}$), which eliminates bus contention.

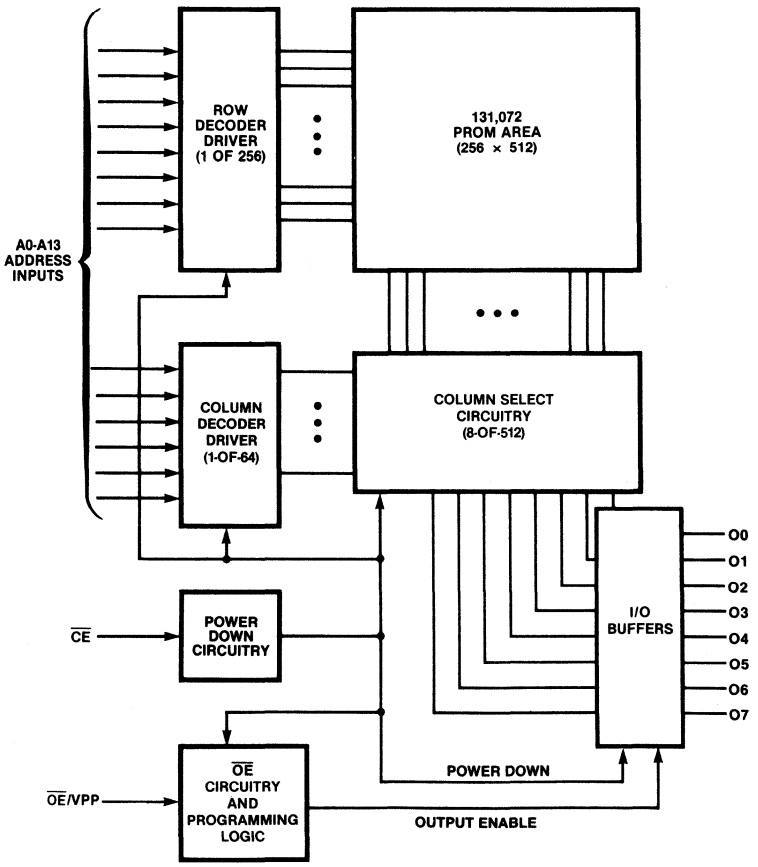
The VT27C128 is manufactured with VLSI's advanced high-performance HCMOS process and is available in a JEDEC-standard 28-pin dual-in-line package.

PIN CONFIGURATION

VT27C128



BLOCK DIAGRAM



PRELIMINARY **VT27C256**

32,768 × 8 STATIC CMOS EPROM

FEATURES

- 32,768 x 8-bit organization
- Current— DC Operating: 5 mA max
  Standby: 10 μA typ
- Totally static operation
- Automatic power-down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- Programming—Voltage: 12.5 V
  Current: 30 mA

DESCRIPTION

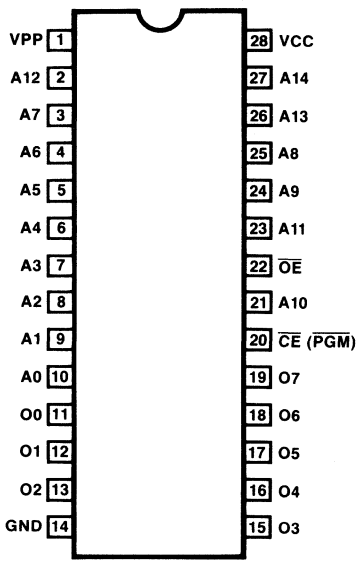
The VT27C256 is a 256K-bit high-performance CMOS Erasable Programmable Read Only Memory that is organized as 32,768 bytes. It is compatible with all microprocessors and similar high-performance applications where high-density storage reprogrammability and simple interfacing are important design considerations.

The VT27C256 has automatic power-down which is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers down and remains in a low-power standby mode. This unique feature provides substantial systems-level power savings. Another function of the VT27C256 is the Output Enable ($\overline{OE}$) which eliminates bus contention.

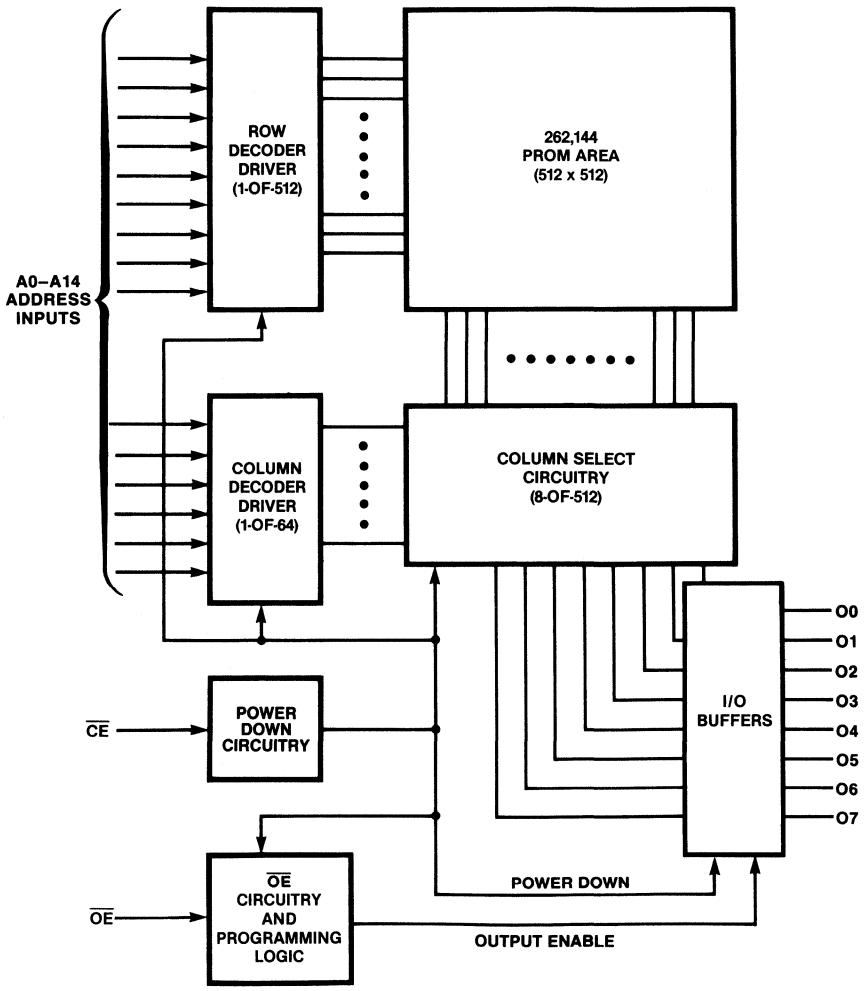
The VT27C256 is manufactured with VTI's advanced high-performance HCMOS process and is available in a JEDEC-standard 28-pin dual in-line package.

PIN CONFIGURATION

VT27C256



BLOCK DIAGRAM



PRELIMINARY **VT27C512**

65,536 x 8 STATIC CMOS EPROM

FEATURES

- 65,536 x 8-bit organization
- Current— Operating: 15 mA max
  — Standby: 1.5 mA max
- Totally static operation
- Automatic power-down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC-approved pinout
- Programming—Voltage: 12.5 V
  —Current: 30 mA

DESCRIPTION

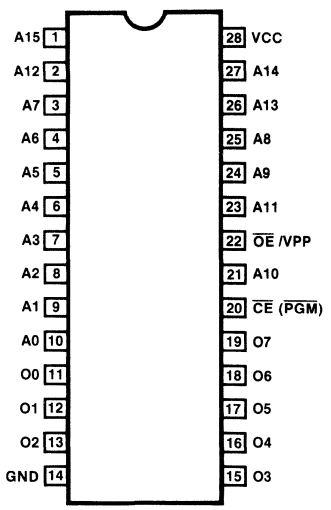
The VT27C512 is a 512K-bit high-performance CMOS erasable programmable read only memory that is organized as 65,536 bytes. It is compatible with all microprocessors and similar high-performance applications where high-density storage reprogrammability and simple interfacing are important design considerations.

The VT27C512 has automatic power-down that is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers down and remains in a low-power standby mode. This unique feature provides substantial systems-level power savings. Another function of the VT27C512 is the Output Enable ($\overline{OE}$), which eliminates bus contention.

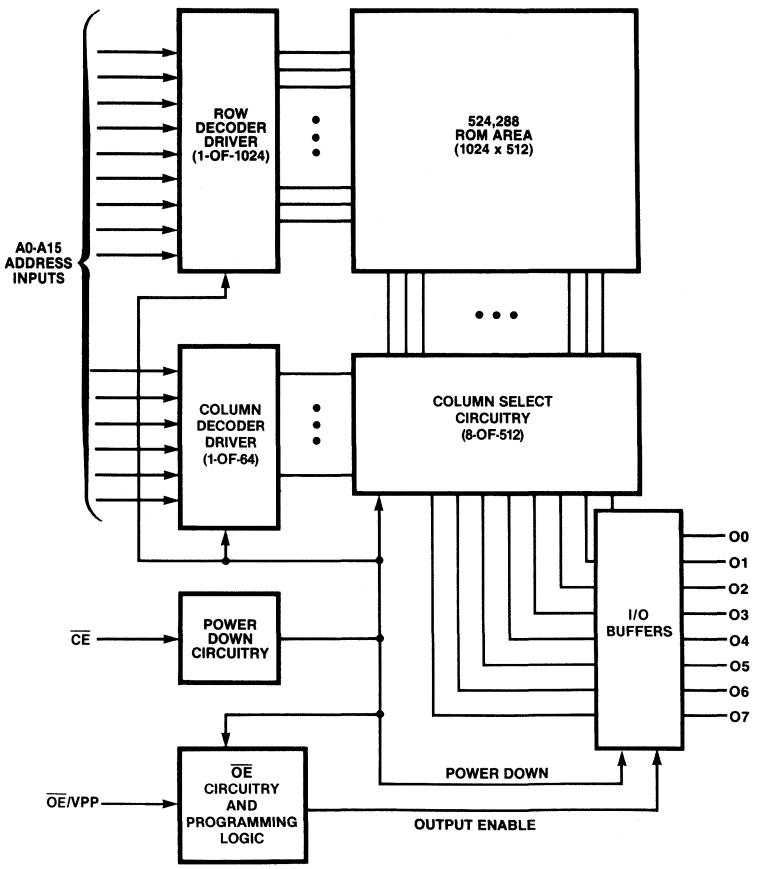
The VT27C512 is manufactured with VLSI's advanced high-performance HCMOS process and is available in a JEDEC-standard 28-pin dual-in-line package.

PIN CONFIGURATION

VT27C512



BLOCK DIAGRAM



VT27C64

8,192 x 8 STATIC CMOS EPROM

FEATURES

- 8,192 x 8-bit organization
- Current—Operating: 15 mA max
  —Standby: 1.5 mA max
- Totally static operation
- Automatic power-down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- Programming—Voltage: 12.5 V
  —Current: 30 mA

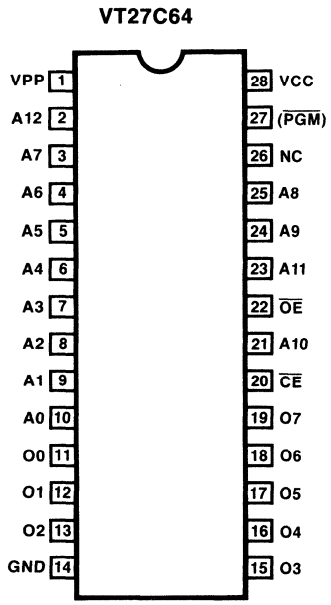
DESCRIPTION

The VT27C64 is a 64K-bit high-performance CMOS Erasable Programmable Read Only Memory that is organized as 8,192 bytes. It is compatible with all microprocessors and similar high-performance applications where high-density storage reprogrammability and simple interfacing are important design considerations.

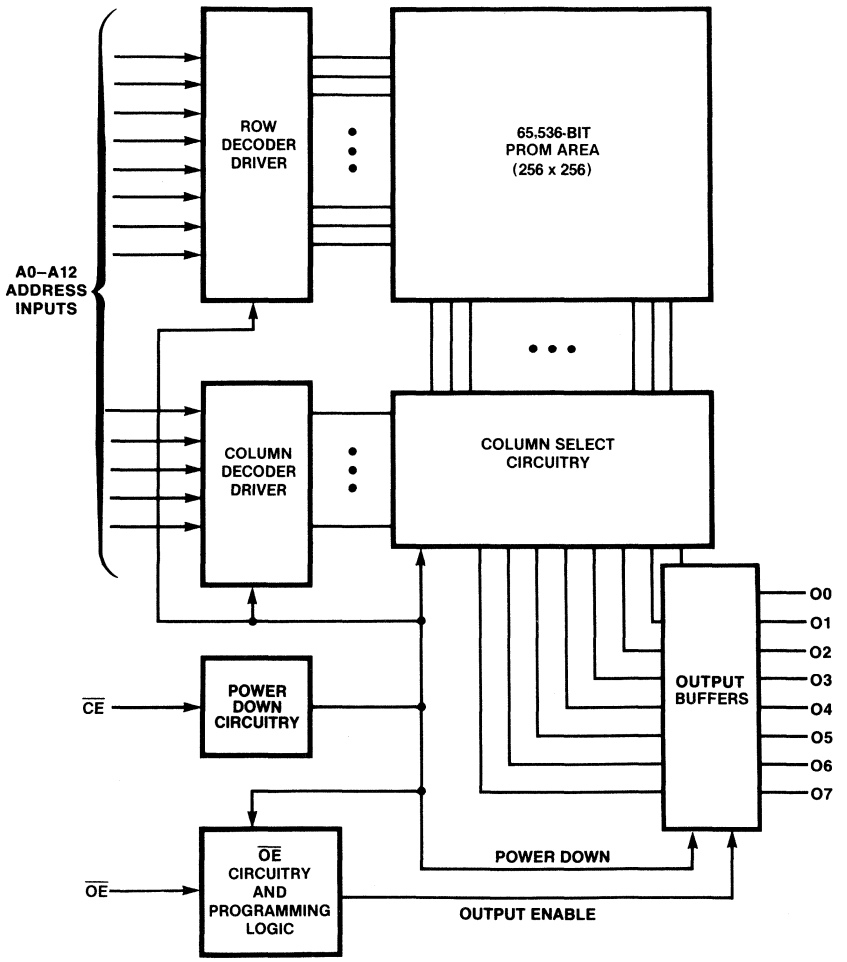
The VT27C64 has automatic power-down which is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers-down and remains in a low-power standby mode. This unique feature provides substantial systems-level power savings. Another function of the VT27C64 is the Output Enable ($\overline{OE}$) which eliminates bus contention.

The VT27C64 is manufactured with VLSI's advanced high-performance HCMOS process and is available in a JEDEC-standard 28-pin dual in-line package.

PIN CONFIGURATION



BLOCK DIAGRAM



VLSI TECHNOLOGY, INC.

SECTION 12

ROM PRODUCTS

Catalog
Product
Descriptions

PRELIMINARY **VT231024**

131,070 × 8 STATIC READ ONLY MEMORY

FEATURES

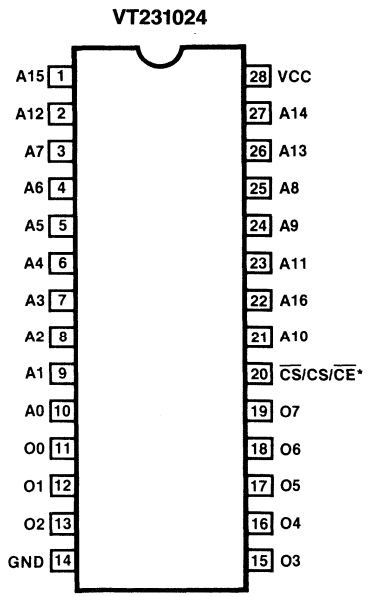
- 131,070 × 8-bit organization
- Access time—150 ns max
- Current—Operating: 100 mA max
  Standby: 20 mA max
- Total static operation
- Static 5 V supply
- Automatic powerdown [$\overline{CE}$]
- Complete TTL compatibility
- 3-State outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- EPROMs accepted as program data input

DESCRIPTION

The VT231024 high performance Read Only Memory is organized 131,070 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

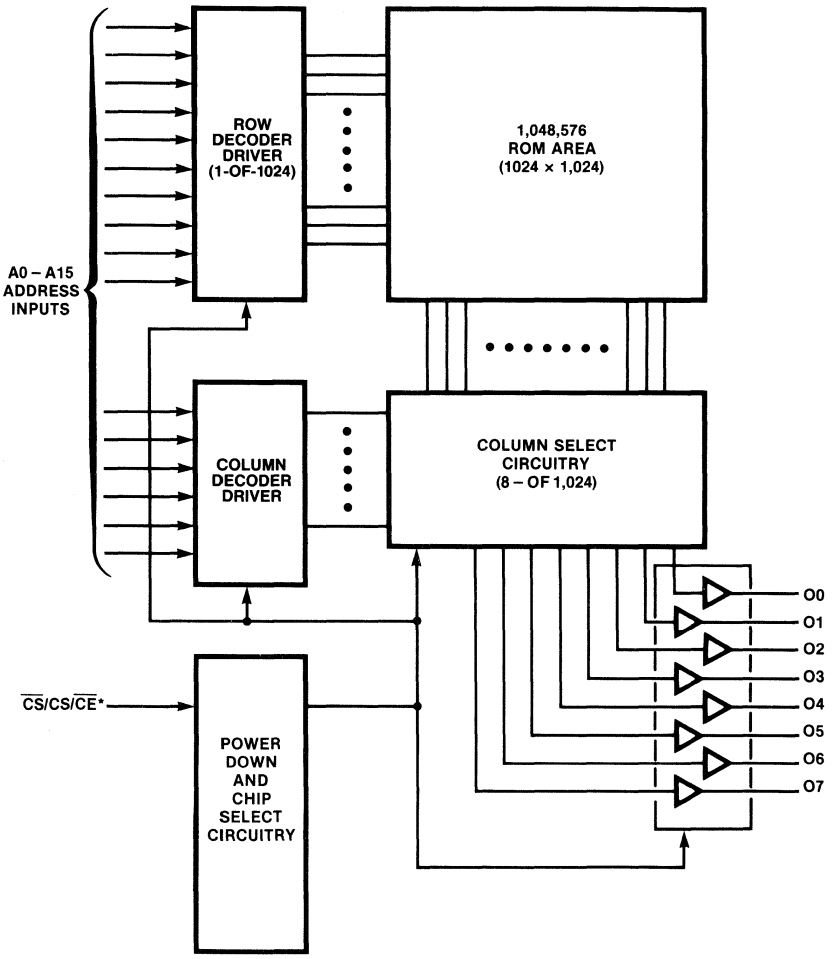
The VT231024 offers automatic power-down with powerdown controlled by the Chip Enable [$\overline{CE}$] input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 80%. Pin 20 may also be programmed as CS (active HIGH or LOW) in order to eliminate bus contention in multiple-bus microprocessor systems.

PIN CONFIGURATIONS



*THIS IS A MASK PROGRAMMABLE OPTION

BLOCK DIAGRAM



PRELIMINARY **VT23512**

65,536 × 8 STATIC READ ONLY MEMORY

FEATURES

- 65,535 × 8-bit organization
- Access time—150 ns max
- Current—Operating: 100 mA max
  Standby: 20 mA max
- Total static operation
- Static 5 V supply
- Automatic powerdown [$\overline{CE}$]
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- EPROMs accepted as program data input

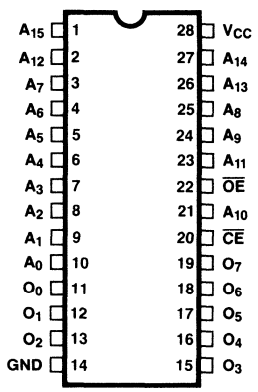
DESCRIPTION

The VT23512 high performance Read Only Memory is organized 65,536 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

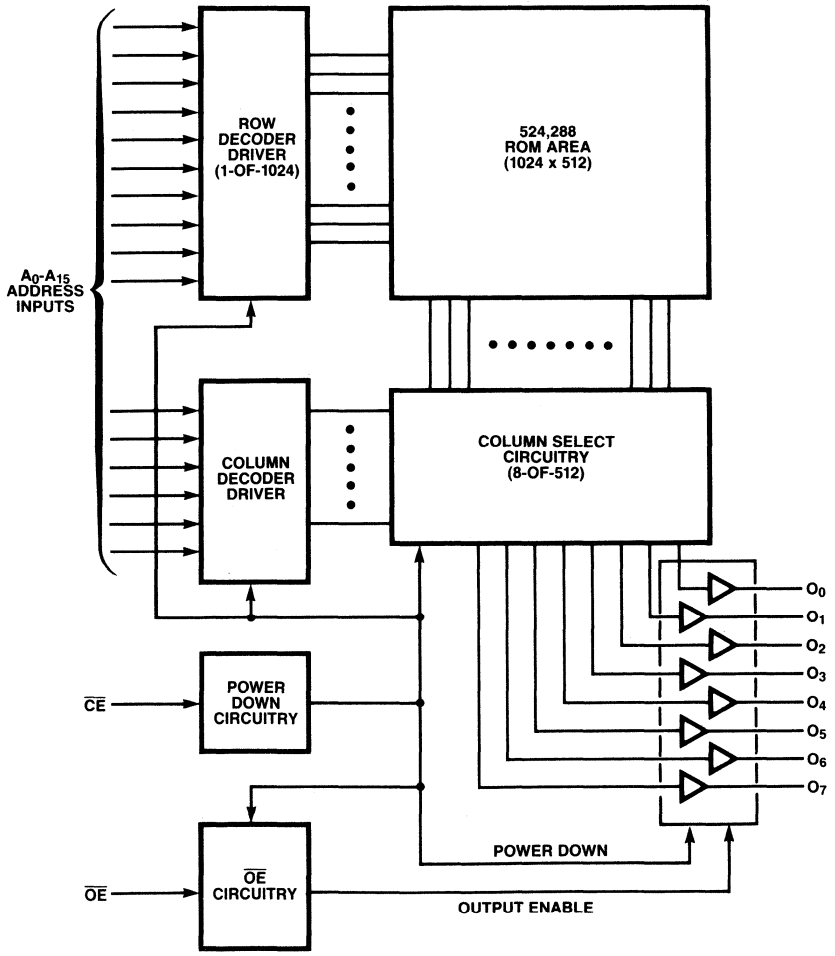
The VT23512 offers automatic power-down with powerdown controlled by the Chip Enable [$\overline{CE}$] input. When $\overline{CE}$ goes HIGH, the device will automatically powerdown and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 80%. The VT23512 also has an Output Enable [$\overline{OE}$] function to eliminate bus contention in multiple-bus microprocessor systems.

PIN CONFIGURATIONS

VT23512



BLOCK DIAGRAM



VLSI TECHNOLOGY, INC.

SECTION 13

GOVERNMENT PRODUCTS

Catalog
Product
Descriptions

GOVERNMENT PRODUCTS

GENERAL

The Government Products Division markets products that are designed and tested to operate under the severe environmental conditions frequently encountered in government and military applications. Its facility has been certified to produce devices that are in conformance with MIL-STD-883C.

The Government Products Division is located at:

10220 South 51st Street
Phoenix, AZ 85044
602/893-8574

CROSS-REFERENCE GUIDE

AMD	VLSI	CYPRESS	VLSI	IDT	VLSI
AM2130	VM2130	CY7C164	VM64KS4	IDT7130S	VM2130
AM2131	VM2131	CY7C166	VM65KS4	IDT7188	VM64KS4
AM99C164	VM64KS4			IDT7198	VM65KS4
AM99C165	VM65KS4				
INTEL	**VLSI**	**INMOS**	**VLSI**	**LATTICE**	**VLSI**
I27C256	VM27C256	IMS1620	VM64KS4	SR64E4	VM65KS4
		IMS1624	VM65KS4	SR64K4	VM64KS4
MOTOROLA	**VLSI**	**NATIONAL**	**VLSI**	**TI**	**VLSI**
MCM6288	VM64KS4	NMC27C256	VM27C256	TMS27C256	VM27C256

PRELIMINARY **VM2130 • VM2131**

1,024 x 8 DUAL PORT RANDOM ACCESS MEMORY

FEATURES

- 100 ns address access time
- Fully static operation
- Fully TTL Compatible
- Interrupt function ($\overline{INT}$): open drain for OR-tied operation
- Easy microprocessor interface
- VM2130—Transparent power-down ($\overline{CE}$)
- VM2131—Non-power-down ($\overline{CS}$)
- Output Enable function ($\overline{OE}$)
- Both ports operate independently.
- Each port accesses entire memory.
- $\overline{BUSY}$ function to handle contention

DESCRIPTION

The VM2130 and VM2131 are 8,192-bit dual-port static random access memories organized 1,024 words by eight bits. They are designed using fully static circuitry and fabricated using n-channel double-poly silicon gate technology.

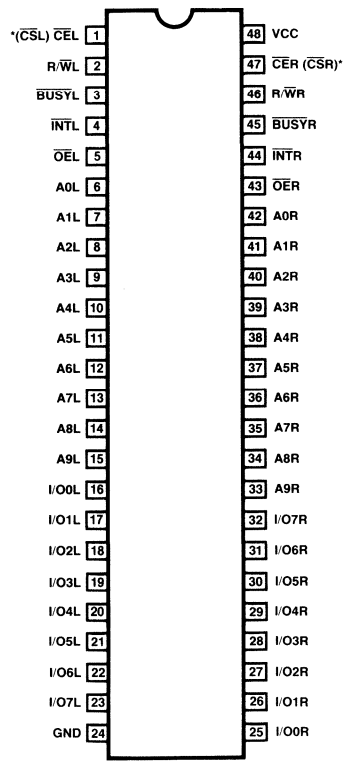
The VM2130 and VM2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The only situation in which contention occurs is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side where the operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

An interrupt function ($\overline{INT}$) is provided to allow communication between systems. This function acts like a writable flag. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. The $\overline{INT}$s have open-drain drivers to allow OR-tied operation.

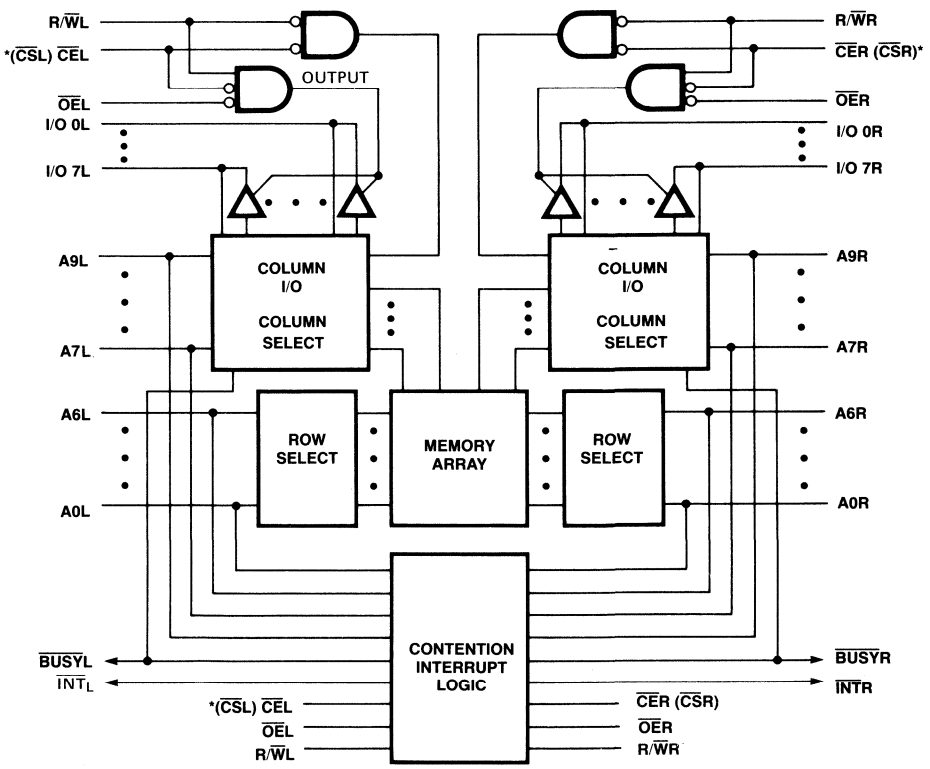
The VM2130 has an automatic power-down feature that is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode.

The VM2131 chip select (no power-down) access has been designed to be faster than its address access so that the chip select decode time does not add to the memory's overall access time. This feature significantly improves system performance.

PIN DIAGRAM



BLOCK DIAGRAM



*Symbol in parentheses applies to VM2131.

VM27C256

32,768 x 8 STATIC CMOS EPROM

FEATURES

- 32,768 x 8-bit organization
- Current—Operating: 30 mA max
  —Standby: 500 μA max
- Total static operation
- Automatic power-down ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- Dual in-line or leadless chip carrier packages
- Programming—Voltage: 12.5 V
  —Current: 30 mA

DESCRIPTION

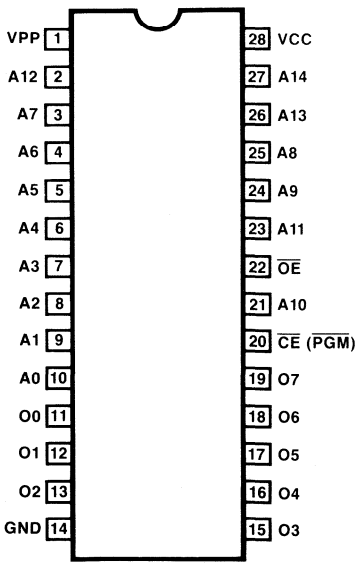
The VM27C256 is a 256K-bit high-performance CMOS erasable programmable read only memory that is organized as 32,768 bytes. It is compatible with all microprocessors and similar high-performance applications in which high-density storage reprogrammability and simple interfacing are important design considerations.

The VM27C256 has automatic power-down that is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device automatically powers down and remains in a low-power standby mode. This unique feature provides substantial system-level power savings. Another function of the VM27C256 is the Output Enable ($\overline{OE}$) signal, which eliminates bus contention.

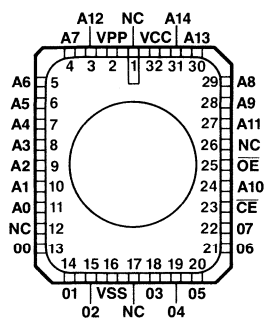
The VM27C256 is manufactured with VLSI's advanced high-performance HCMOS process and is available in both JEDEC-standard 28-pin side-brazed and 32-pin leadless chip carrier packages.

PIN DIAGRAMS

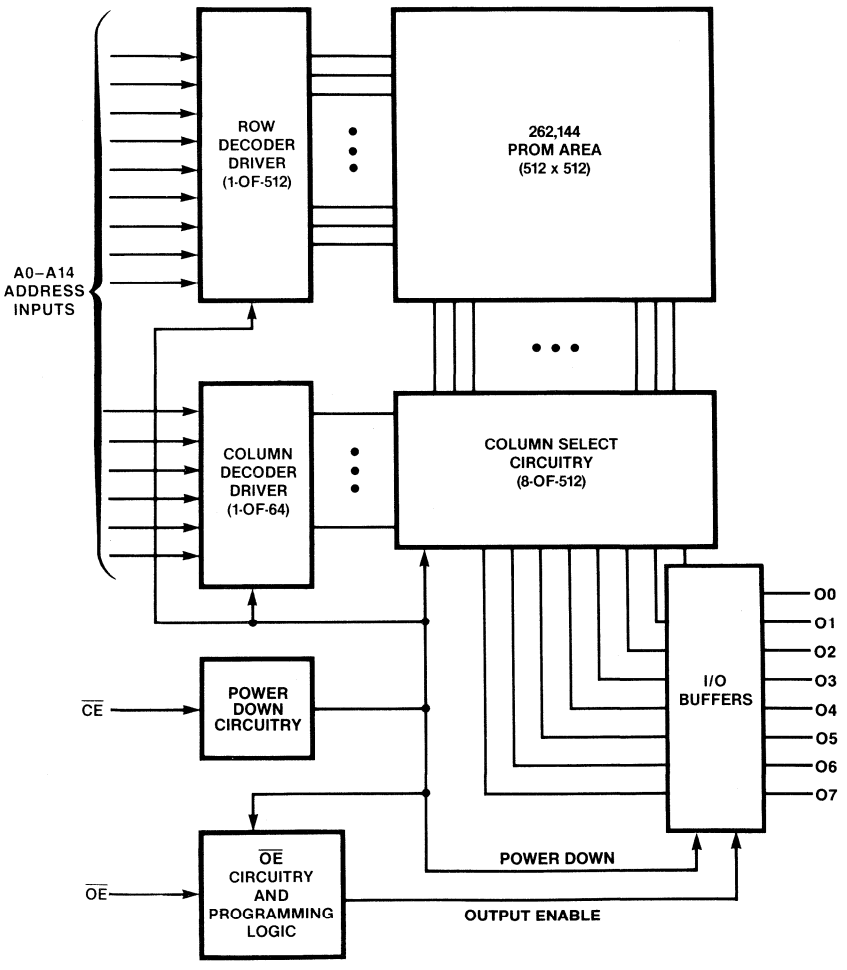
VM27C256



VM27C256



BLOCK DIAGRAM



VLSI TECHNOLOGY, INC.

PRELIMINARY **VM64KS4/VM65KS4**

16,384 x 4 HIGH-SPEED 64K STATIC RAM

FEATURES

- 16,384 x 4-bit organization
- Access time—45 ns max
- Current—Operating: 120 mA max
  —Standby: 30 mA max
- Total static operation
- Single 5 V supply
- Output enable ($\overline{OE}$) function (VM65KS4)
- Complete TTL compatibility
- 3-state I/O
- 22-, 24-, 28-pin JEDEC-approved pinout

DESCRIPTION

The VM64KS4 and VM65KS4 are high-speed static random access memories organized as 16,384 words by four bits.

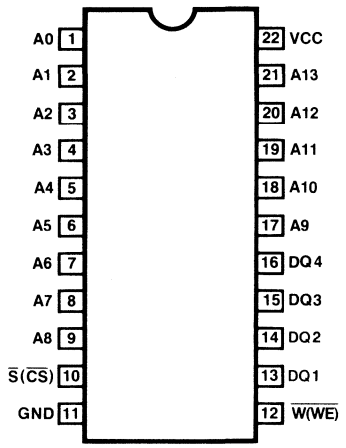
The devices are fabricated in CMOS technology and achieve access times of 45 ns with a maximum power consumption of 660 mW. The high speed of the VM64KS4 and VM65KS4 enable them to replace bipolar and fast NMOS memories in many applications.

The fully static circuits require no clocks or refreshing for operation. The VM64KS4/VM65KS4 provide equal access and cycle times for ease of use. The VM65KS4 also features an output enable function that eliminates any potential bus contention.

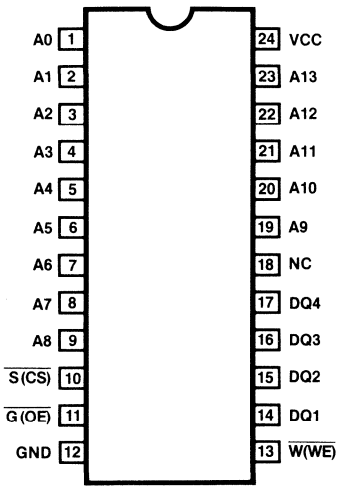
The device operates from a single 5 V power supply and is completely TTL compatible.

PIN DIAGRAMS

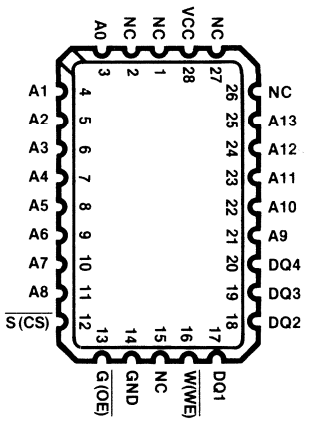
VM64KS4



VM65KS4



VM64KS4

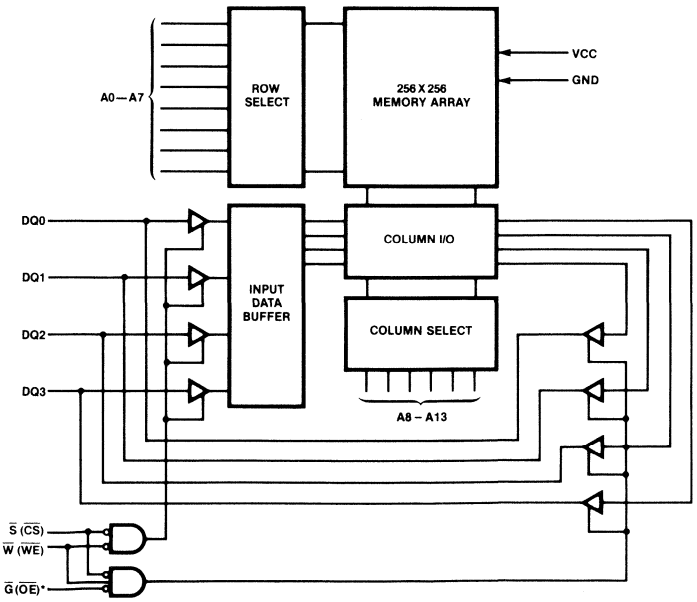


PIN DESCRIPTIONS

A0 - A13	Address
DQ0 - DQ3	Data Input/Output
$\overline{S}(\overline{CS})$	Chip Select
$\overline{G}(\overline{OE})$*	Output Enable*
$\overline{W}(\overline{WE})$	Write Enable
VCC	Power
GND	Ground

*VM65KS4 only

BLOCK DIAGRAM



VLSI TECHNOLOGY, INC.

SECTION 14

PROGRAMMABLE LOGIC PRODUCTS

Catalog
Product
Descriptions

CROSS-REFERENCE GUIDE

MMI	VLSI
PAL10H8CN	VP16V8E-35PC
PAL10L8CN	VP16V8E-35PC
PAL12H6CN	VP16V8E-35PC
PAL14H4CN	VP16V8E-35PC
PAL14L4CN	VP16V8E-35PC
PAL16H2CN	VP16V8E-35PC
PAL16L8CN	VP16V8E-35PC
PAL16L8ACN	VP16V8E-25PC
PAL16L8A-2CN	VP16V8E-35PC
PAL16L8B-2CN	VP16V8E-25PC
PAL16R4CN	VP16V8E-35PC
PAL16R4ACN	VP16V8E-25PC
PAL16R4A-2CN	VP16V8E-35PC
PAL16R4B-2CN	VP16V8E-25PC
PAL16R6CN	VP16V8E-35PC
PAL16R6ACN	VP16V8E-25PC
PAL16R6A-2CN	VP16V8E-35PC
PAL16R6B-2CN	VP16V8E-25PC
PAL16R8CN	VP16V8E-35PC
PAL16R8ACN	VP16V8E-25PC
PAL16R8A-2CN	VP16V8E-35PC
PAL16R8B-2CN	VP16V8E-25PC
PAL14L8CN	VP20V8E-35PC
PAL16L6CN	VP20V8E-35PC
PAL18L4CN	VP20V8E-35PC
PAL20L2CN	VP20V8E-35PC
PAL20L8ACN	VP20V8E-25PC
PAL20R4ACN	VP20V8E-25PC
PAL20R6ACN	VP20V8E-25PC
PAL20R8ACN	VP20V8E-25PC

CYPRESS	VLSI
PAL16L8APC	VP16V8E-25PC
PAL16L8A-2PC	VP16V8E-35PC
PAL16R4APC	VP16V8E-25PC
PAL16R4A-2PC	VP16V8E-35PC
PAL16R6APC	VP16V8E-25PC
PAL16R6A-2PC	VP16V8E-35PC
PAL16R8APC	VP16V8E-25PC
PAL16R8A-2PC	VP16V8E-35PC

NATIONAL	VLSI
PAL10H8NC	VP16V8E-35PC
PAL10H8ANC	VP16V8E-25PC
PAL10L8NC	VP16V8E-35PC
PAL10L8ANC	VP16V8E-25PC
PAL12H6NC	VP16V8E-35PC
PAL12H6ANC	VP16V8E-25PC
PAL12L6NC	VP16V8E-35PC
PAL12L6ANC	VP16V8E-25PC
PAL14H4NC	VP16V8E-35PC
PAL14H4ANC	VP16V8E-25PC
PAL14L4NC	VP16V8E-35PC
PAL14L4ANC	VP16V8E-25PC
PAL16H2NC	VP16V8E-35PC
PAL16H2ANC	VP16V8E-25PC
PAL16L2NC	VP16V8E-35PC
PAL16L2ANC	VP16V8E-25PC
DMPAL16L8NC	VP16V8E-35PC
DMPAL16L8ANC	VP16V8E-25PC
DMPAL16R4NC	VP16V8E-35PC
DMPAL16R4ANC	VP16V8E-25PC
DMPAL16R6NC	VP16V8E-35PC
DMPAL16R6ANC	VP16V8E-25PC
DMPAL16R8NC	VP16V8E-35PC
DMPAL16R8ANC	VP16V8E-25PC

AMD	VLSI
AMPAL16H8PC	VP16V8E-35PC
AMPAL16H8APC	VP16V8E-25PC
AMPAL16HD8PC	VP16V8E-35PC
AMPAL16HD8APC	VP16V8E-25PC
AMPAL16L8PC	VP16V8E-35PC
AMPAL16L8APC	VP16V8E-25PC
AMPAL16LD8PC	VP16V8E-35PC
AMPAL16LD8APC	VP16V8E-25PC
AMPAL16R4PC	VP16V8E-35PC
AMPAL16R4APC	VP16V8E-25PC
AMPAL16R6PC	VP16V8E-35PC
AMPAL16R6APC	VP16V8E-25PC
AMPAL16R8PC	VP16V8E-35PC
AMPAL16R8APC	VP16V8E-25PC

TI	VLSI
PAL16L8ACN	VP16V8E-25PC
PAL16L8A-2CN	VP16V8E-35PC
TIBPAL16L8-25CN	VP16V8E-25PC
PAL16R4ACN	VP16V8E-25PC
PAL16R4A-2CN	VP16V8E-35PC
TIBPAL16R4-25CN	VP16V8E-25PC
PAL16R6ACN	VP16V8E-25PC
PAL16R6A-2CN	VP16V8E-35PC
TIBPAL16R6-25CN	VP16V8E-25PC
PAL16R8ACN	VP16V8E-25PC
PAL16R8A-2CN	VP16V8E-35PC
TIBPAL16R8-25CN	VP16V8E-25PC
PAL20L8ACN	VP20V8E-25PC
PAL20L8A-2CN	VP20V8E-35PC
PAL20R4ACN	VP20V8E-25PC
PAL20R4A-2CN	VP20V8E-35PC
PAL20R6ACN	VP20V8E-25PC
PAL20R6A-2CN	VP20V8E-35PC
PAL20R8ACN	VP20V8E-25PC
PAL20R8A-2CN	VP20V8E-35PC

LATTICE	VLSI
GAL16V8-25CP	VP16V8E-25PC
GAL16V8-35CP	VP16V8E-35PC
GAL20V8-25CP	VP20V8E-25PC
GAL20V8-35CP	VP20V8E-35PC

™GAL is a trademark of Lattice Corp.

VP16RP8M • VP20RP8M

CMOS MASK PROGRAMMABLE LOGIC ARRAY

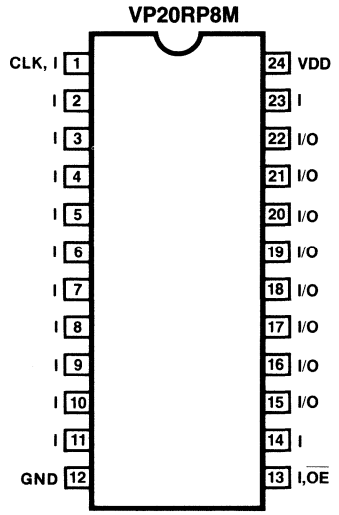
FEATURES

- Low cost Mask Programmable Logic Array
- Pin compatible with industry standard HALs/PALs,* and GALs†
- Semicustom replacement for 7400 and 4000 series SSI/MSI
- High Performance—25 ns tPD max
  35 ns option
- Operating current—45 mA/58 mA max
- Complete TTL or CMOS compatibility
- Improved testability through register pre-load
- Industry standard 300 mil 20- and 24-pin packages
- Fast prototype turnaround

DESCRIPTION

The VP16RP8M and VP20RP8M combine bipolar speed and CMOS power dissipation in a pin-compatible replacement of industry standard programmable logic arrays. Devices which may be replaced by the VP16RP8M and VP20RP8M are listed in Table 1. Customer logic equations are implemented through a metal mask option to make customer specified interconnects in the AND and OR planes, rather than using the fuses or EPROM cells that are found in field programmable logic arrays. Metal is the programming medium because it is one of the last steps in the fabrication process. Thus, lead times to prototypes and production are minimized. Through utilization of advanced CMOS processing and automated mask generation techniques, VLSI Technology has developed a design automation system to create custom masks directly from customer logic equations or programmed PALs or GALs. The VP16RP8M-25 and VP20RP8M-25 offer 25 ns delay times, at up to one-third the power of the equivalent bipolar devices. These parts are compatible in all respects with the 20/24-pin AND and OR array structures incorporated in HAL/PAL devices and VLSI Technology's electrically erasable programmable logic devices, the Generic Array Logic (GAL) devices, VP16V8E and VP20V8E.

PIN DIAGRAM



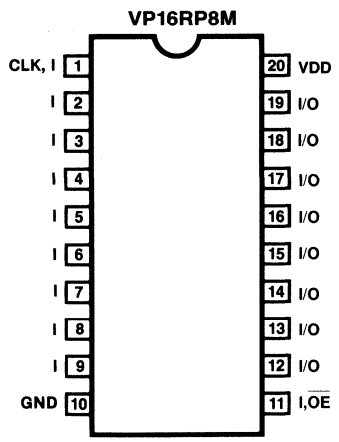


TABLE 1: REPLACEMENT GUIDE

VLSI	Cross Reference
VP16RP8M-25	PAL16L8A, PAL16R8A, PAL16R6A, PAL16R4A, PAL16L8B-2, PAL16R8B-2, PAL16R6B-2, PAL16R4B-2, PAL16P8A, PAL16RP8A, PAL16RP6A, PAL16RP4A, PAL16L8, PAL16R8, PAL16R6, PAL16R4, PAL16L8A-2, PAL16R8A-2, PAL16R6A-2, PAL16R4A-2, PAL16L8B-4, PAL16R8B-4, PAL16R6B-4, PAL16R4B-4, PAL10H8, PAL12H6, PAL14H4, PAL16H2, PAL16C1, PAL10L8, PAL12L6, PAL14L4, PAL16L2, VP16V8E-25, VP16V8E-35
VP20RP8M-25	PAL6L16A, PAL8L14A, PAL20L8A, PAL20R8A, PAL20R6A, PAL20R4A, PAL20L10A, PAL20L8A-2, PAL20R8A-2, PAL20R6A-2, PAL20R4A-2, PAL20L10, PAL12L10, PAL14L8, PAL16L6, PAL18L4, PAL20L2, PAL20C1, VP20V8E-25, VP20V8E-35
VP16RP8M-35	PAL16L8B-4, PAL16R8B-4, PAL16R6B-4, PAL16R4B-4, PAL16L8A-2, PAL16R8A-2, PAL16R6A-2, PAL16R4A-2, PAL16L8, PAL16R8, PAL16R6, PAL16R4, PAL16L8A-4, PAL16R8A-4, PAL16R6A-4, PAL16R4A-4, PAL10H8, PAL12H6, PAL14H4, PAL16H2, PAL16C1, PAL10L8, PAL12L6, PAL14L4, PAL10H8-2, PAL12H6-2, PAL14H4-2, PAL16H2-2, PAL16C1-2, PAL10L8-2, PAL12L6-2, PAL14L4-2, PAL16L2-2, VP16V8E-35
VP20RP8M-35	PAL2L8A-2, PAL20R8A-2, PAL20R6A-2, PAL20R4A-2, PAL12L10, PAL14L8, PAL16L6, PAL18L4, PAL20L2, PAL20C1, PAL20L10, VP20V8E-35

PIN DESCRIPTIONS

I	Input
I/O	Input or Output
CLK	Register Clock
$\overline{OE}$	Output Enable Bar

*HAL and PAL are registered trademarks of Monolithic Memories, Inc. †GAL is a trademark of Lattice Semiconductor Corporation.

VP16V8E • VP20V8E

GENERIC ARRAY LOGIC

FEATURES

- VP16V8E replaces most 20-pin bipolar PAL® devices
- VP20V8E replaces most 24-pin bipolar PAL devices
- 24 mA output drive
- High performance CMOS technology —25 ns and 35 ns maximum propagation delays
- EE technology—
  Reconfigurable logic
  Reprogrammable fuses
  100% testable
- Generic architecture—
  Flexible output macrocells allow
  User defined architectures
  Single-device inventory
  System design flexibility
- Electronic signature word allows user-programmable ID code and revision identification for inventory control
- Security cell prevents logic copying
- Register preload for complete testability
- Power-on reset for all registers
- High-speed programming algorithm
- JEDEC approved TTL compatible pin-outs

DESCRIPTION

The VLSI Electrically Erasable GAL* devices, VP16V8E and VP20V8E, combine a high performance CMOS process with electrically erasable floating gate technology. This proven memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at reduced power levels.

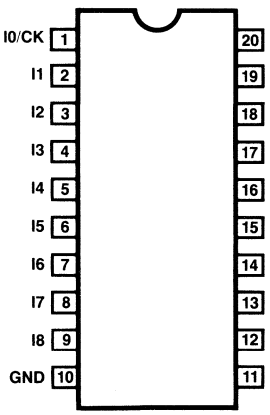
Two speed options are available, the VP16V8E-25 and VP20V8E-25 offer industry standard 25 ns maximum propagation delays. For less speed-critical applications, the VP16V8E-35 and VP20V8E-35 have a maximum propagation delay of 35 ns.

The innovative output logic macrocell used in these devices allows non-standard architectures, such as 16R5, to be created in addition to most industry-standard 20-pin configurations and many of the industry-standard 24-pin configurations.

Unique test circuitry and reprogrammable cells allow complete ac, dc, fuse and functionality testing during manufacture. This results in virtually 100% field programmability and functionality yield of VLSI GAL devices. In addition, electronic signature is available to provide positive device identification and a security circuit is built in, providing the user's proprietary circuit with copy protection.

The GAL device fuse map is logically equivalent to the industry standard PAL devices and is programmed with readily available hardware and software tools. VLSI guarantees 100 erase/write cycles and data retention exceeding 10 years.

PIN DIAGRAM FOR PAL REPLACEMENTS: VP16V8E



VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
F7	I11	I13	I15	F7	B1	B3	F1
F6	F5	I12	I14	F6	F5	B2	B5
F5	F4	F3	I13	F5	F4	F3	B4
F4	F3	F2	F1	F4	F3	F2	B3
F3	F2	F1	F0	F3	F2	F1	B2
F2	F1	F0	I12	F2	F1	F0	B1
F1	F0	I11	I11	F1	F0	B1	B0
F0	I10	I10	I10	F0	B0	B0	F0
I9	I9	I9	I9	$\overline{G}$($\overline{OE}$)	$\overline{G}$($\overline{OE}$)	$\overline{G}$($\overline{OE}$)	I9
10L8 10H8 10P8	12L6 12H6 12P6	14L4 14H4 14P4	16L2 16H2 16P2	16R8 16RP8	16R6 16RP6	16R4 16RP4	16L8 16H8 16P8
GAL™ 16V8							

PIN NAMES: VP16V8E

I0–I15	Input	$\overline{G}$ ($\overline{OE}$)	Output Enable
CK	Clock Input		
B0–B5	Bi-Directional	VDD	Power (5 V)
F0–F7	Output	GND	Ground

®PAL is a registered trademark of Monolithic Memories Inc.
*GAL is a trademark of Lattice Semiconductor.

VLSI TECHNOLOGY, INC.

SECTION 15

SALES OFFICES, DESIGN CENTERS, AND DISTRIBUTORS

Catalog
Product
Descriptions

VLSI TECHNOLOGY, INC.

VLSI CORPORATE OFFICES

CORPORATE HEADQUARTERS • ASIC AND MEMORY PRODUCTS • VLSI Technology, Inc. • 1109 McKay Drive • San Jose, CA 95131 • 408-434-3100

APPLICATION SPECIFIC LOGIC AND GOVERNMENT PRODUCTS • VLSI Technology, Inc. • 10220 South 51st Street • Phoenix, AZ 85044 • 602-893-8574/VLSI

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BOSTON
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FAX 617-657-6420

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1350 Remington Rd., Stes. A-B
Schaumburg, IL 60195
312-310-9595
FAX 312-310-9632

DALLAS
850 E. Arapaho Rd., Ste. 270
Richardson, TX 75081
214-231-6716
FAX 214-669-1413

PRINCETON
101 Morgan Lane, Ste. 380
Plainsboro, NJ 08536
609-799-5700
FAX 609-799-5720

SAN JOSE
2235 Qume Dr.
San Jose, CA 95131
408-943-0261
FAX 408-263-2511
TELEX 278807
MAIL 1109 McKay Dr.
San Jose, CA 95131

SANTA ANA
1751 E. Garry Ave., Ste. A
Santa Ana, CA 92705
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FAX 714-250-9041

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TELEX 825135 VLSI UK G
FAX 44-908-670027

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91120 Palaiseau-France
33-1-64470479
TELEX 600759F
FAX 33-1-644704880

GERMANY
Rosenkavalierplatz 10
D-8000 Munich 81
West Germany
49-89-926905-0
TELEX 521 4279-VLSI D
FAX 49-89-92690545

ASIA

JAPAN
Shuwa-Kioicho Tbr Blvd., Room 816
5-7 Kojimati, Chiyoda-Ku
Tokyo, Japan 102
81-3-239-5212
FAX 81-3-239-5215

VLSI SALES OFFICES

ATLANTA
3020 Holcomb Bridge Rd., Ste. 110
Norcross, GA 30071
404-446-1326

BALTIMORE
P.O. Box 289
124 Maryland, Rte. 3 N.
Millersville, MD 21108
301-987-8777
FAX 301-987-8779

FORT LAUDERDALE
2200 Park Central N., Ste. 600
Pompano Beach, FL 33064
305-971-0404
FAX 305-971-2086

KING OF PRUSSIA
1012 W. Ninth Ave.
King of Prussia, PA 19406
215-265-8690

LONGMONT
P.O. Box 1432
Longmont, CO 80501
303-440-4778

LOS ANGELES
225 W. Broadway, Ste. 500
Glendale, CA 91204
818-995-2404

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5871 Cedar Lake Rd., Ste. 9
St. Louis Park, MN 55416
612-545-1490

NEW HAVEN
60 Church Street
Yalesville, CT 06492
203-265-6698

PHOENIX
10220 S. 51st St.
Phoenix, AZ 85044
602-893-8574
FAX 602-893-0807

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Portland, OR 97223
503-244-9882
FAX 503-244-9880

TAMPA
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Clearwater, FL 33516
813-443-5797
FAX 813-443-5674

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ARIZONA
SYSTEM SALES OF ARIZONA
Tempe, 602-829-9338

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BESTRONICS
San Diego, 619-693-1111
JONES AND MCGEOY SALES
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EMERGING TECHNOLOGY
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EMERGING TECHNOLOGY
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IOWA
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ELECTRI-REP
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L-MAR ASSOC.
Rochester, 716-323-1000
TWX 510-253-0942
L-MAR ASSOC.
E. Syracuse, 315-437-7779
TRI-TEK ASSOCIATES
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ELECTRONIC MFGS'. AGENTS
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SAI MARKETING CORP.
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SAI MARKETING CORP.
Shaker Heights, 216-751-3633

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Tulsa, 918-494-0765

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MICRO SALES
Aloha, 503-642-1818

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LOGIC 1 SALES
Houston, 713-981-0233
LOGIC 1 SALES
Richardson, 214-234-0765
LOGIC 1 SALES
Fort Worth, 817-336-2192

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613-729-0023
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514-697-0804

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(1) 3043.82.33

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bit electronic AG
München, Germany
089/4180 07-0
SE SPEZIAL-ELECTRONIC KG
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0 5722/20 32

HOLLAND
DIODE
Houten, Holland
(0 34 03) 912 34

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Marlton, 609-596-8000

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